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NEC:LunarEagle

MSI:MS-7420N1

Version:0B



CPU: Conroe family processors /WolfDale/Yorkfield in LGA775 Package.

System Chipset:

Intel EagleLake-Q+Intel ICH10-DO

On Board Device:

BIOS -- SPI Flash 32M

LAN --INTEL 82567LM Boazman

Super I/O -- SMSC5617C

AUDIO -- Realtek HD ALC262VD

Clock GEN-IDTCV184-2

TPM-SLB 9635 TT1.2

Main Memory:

Due-channel DDR-III * 2 (1066MHZ)

Intersil PWM:


Controller: Intersil ISL6334 (3 Phases)

Expansion Slots:

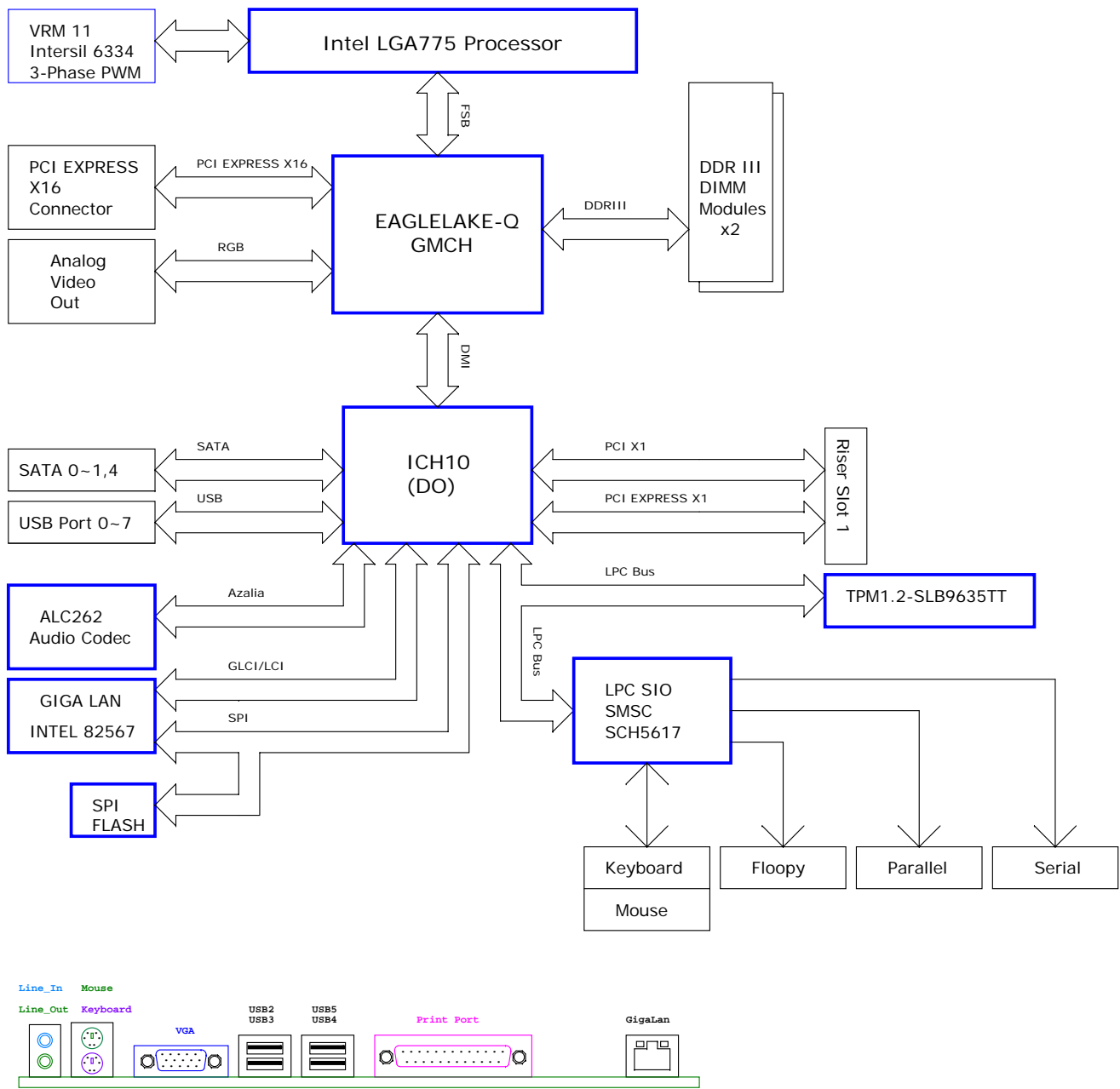
PCI-E(X16) Slot *1

Riser Slot :(PCIx1/PCI-E(x1)x1)

MS-6497N1	ERP Number	Function
MS-7420-0B	601-7420-B10	Mainboard
MS-4046-2A	604-4046-020	Power Button/LED board
MS-4085-10	604-4085-020	Front Audio Board
MS-4048-40	604-4048-050	Front USB Board
MS-4121-10	604-4121-010	Riser Card

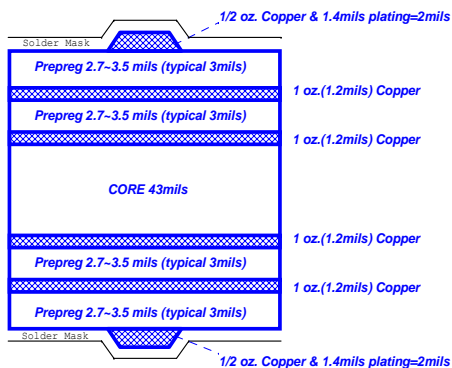
 MICRO-START INT'L CO.,LTD.		
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Block Diagram



Board Stack-up (6 layers)

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
Differential Clock : 18/4/10/4/18

Example Fab Drawing Note (1080 Prepreg PCB)


Trace Width (mils)	Differential Spacing (mils)	Target Impedance	Tolerance
4.0	NA	50-ohm, single-ended	15%
6.5	NA	40-ohm, single-ended	15%
7.5	NA	30-ohm, single-ended	15%
9.5	NA	32-ohm, single-ended	15%
3.9	8.1	95-ohm, differential	20%, reference only
4.5	7.5	90-ohm, differential	20%, reference only

Eaglelake(GMCH) Impedance Requirements by Interface

Interface	Impedance Required
FSB (All)	4x signals 42-ohm, others 50-ohm, single-ended
Controller Link	50-ohm, single-ended
DDR2 (DQ, DQS, DM, CLK, CLK#)	40-ohm, single-ended
DDR2 (Control)	43-ohm, single-ended
DDR2 (Command)	33-ohm, single-ended
DDR3 (CLK, CLK#)	36-ohm, single-ended
DDR3 (DQ, DQS, DM)	20/37-ohm, single-ended
DDR3 (Control)	36-ohm, single-ended
DDR3 (Command)	32-ohm, single-ended
PCI Express, DMI	95-ohm, differential
VGA	97-ohm, single-ended at MCH breakout, then 50-ohm, single-ended to VGA connector

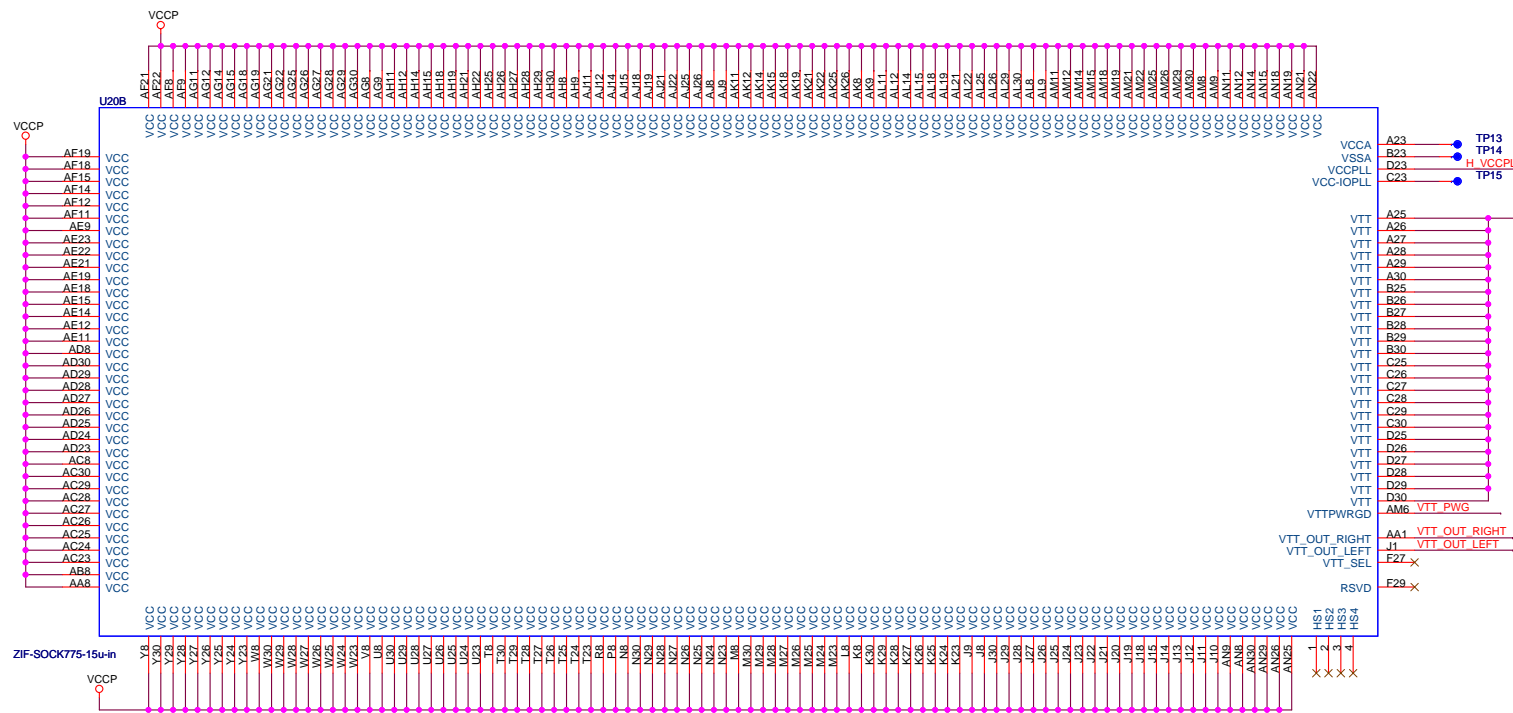
ICH10 Impedance Requirements by Interface

Interface	Impedance Required
PCI	50-ohm, single-ended
Controller Link	50-ohm, single-ended
Miscellaneous	50-ohm, single-ended
PCI Express, DMI	95-ohm, differential
SATA	95-ohm, differential
USB	90-ohm, differential

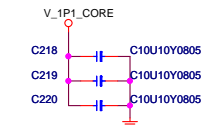
 MICRO-START INTL CO., LTD.		
Title BLOCK DIAGRAM		
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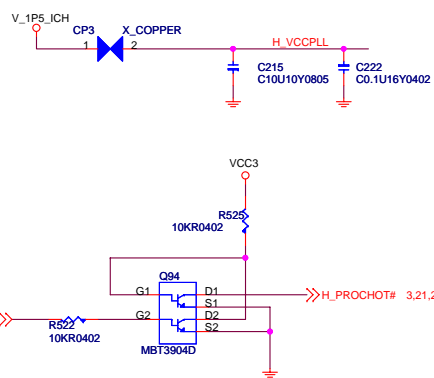
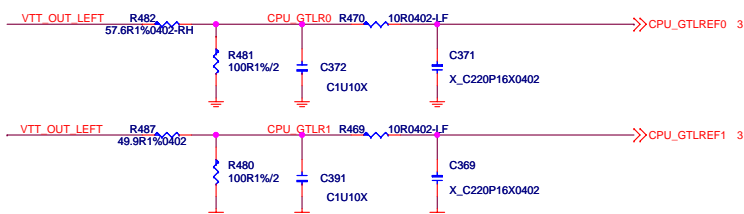
BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)
1	0	0	333 MHZ (1333)



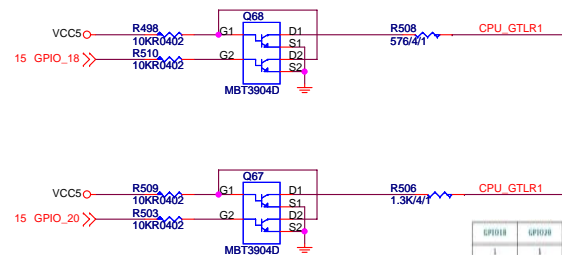
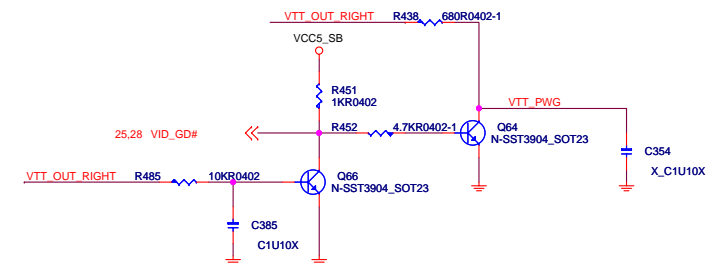
BIOS writers Guide
PDG:page109



CAPS FOR FSB GENERIC

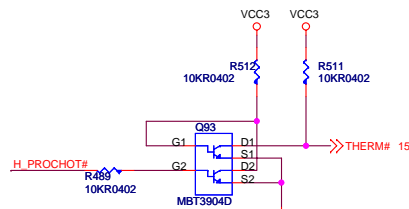


VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

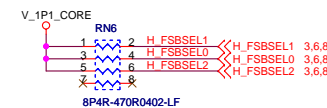


PLACE AT CPU END OF ROUTE

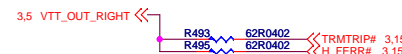
Q67	Q68	Ratio Test
1	1	0.67
1	0	0.65
0	1	0.63
0	0	0.61

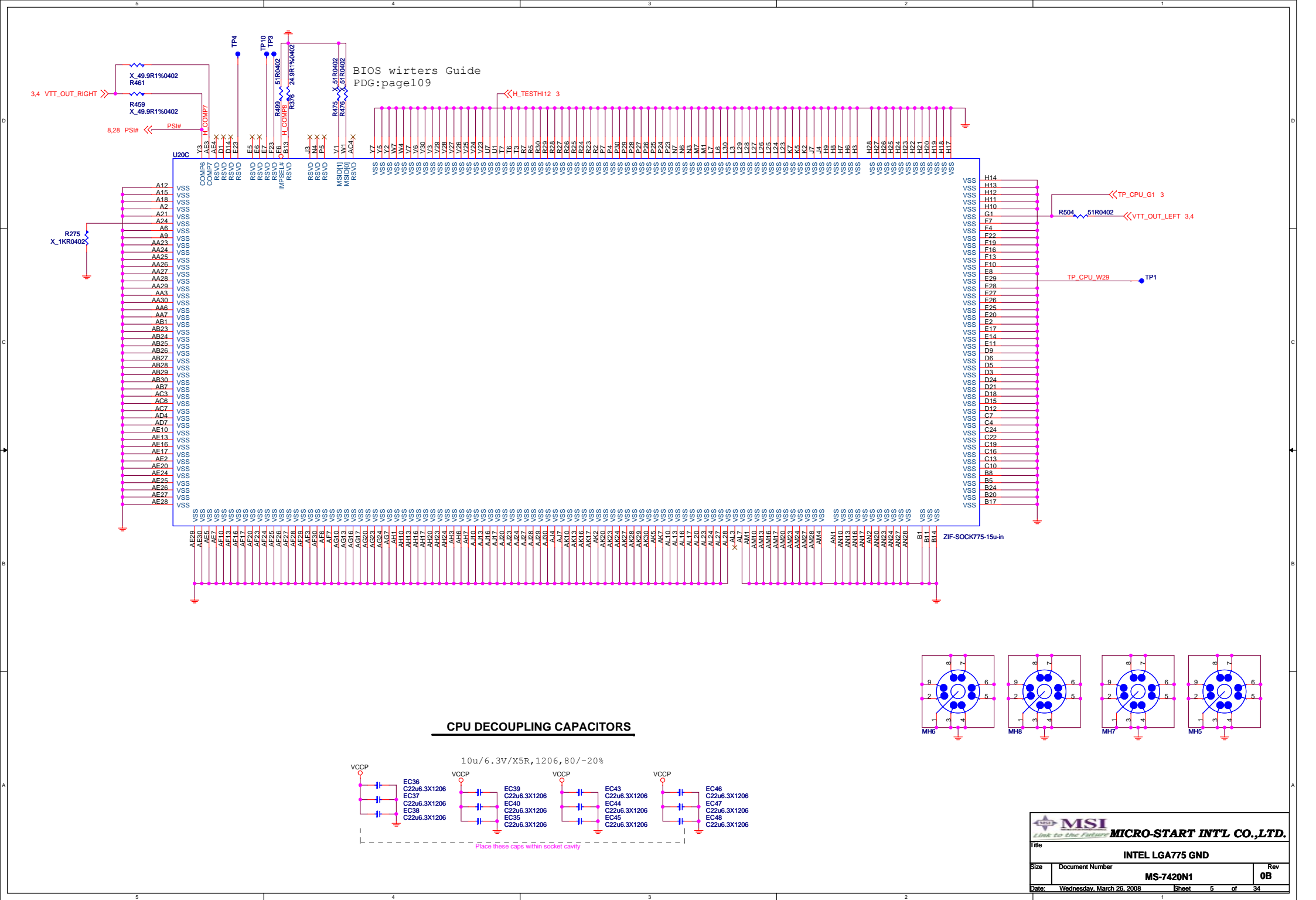


FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS
AND CEDAR MILL ARE SUPPORTED



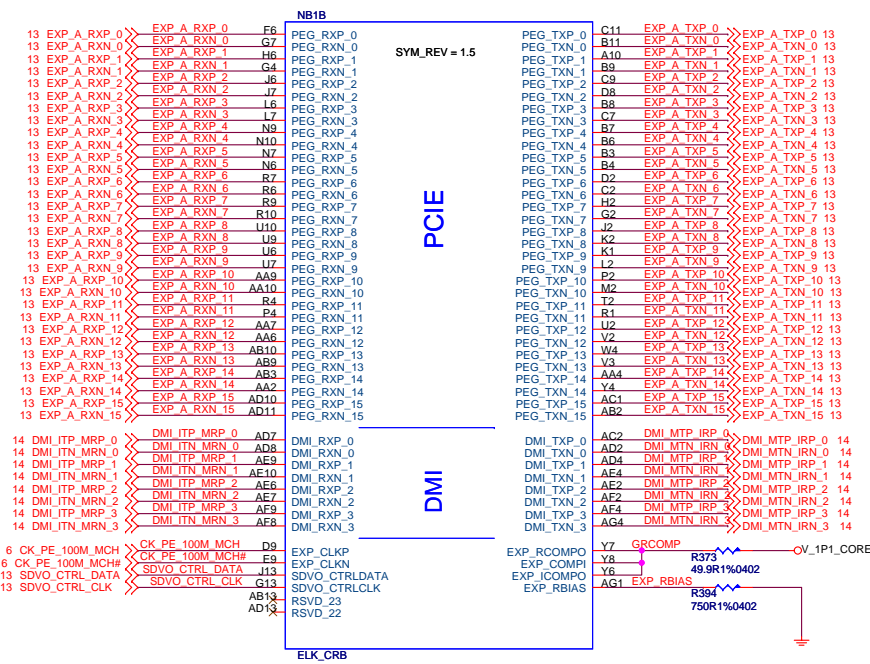
PLACE AT ICH END OF ROUTE

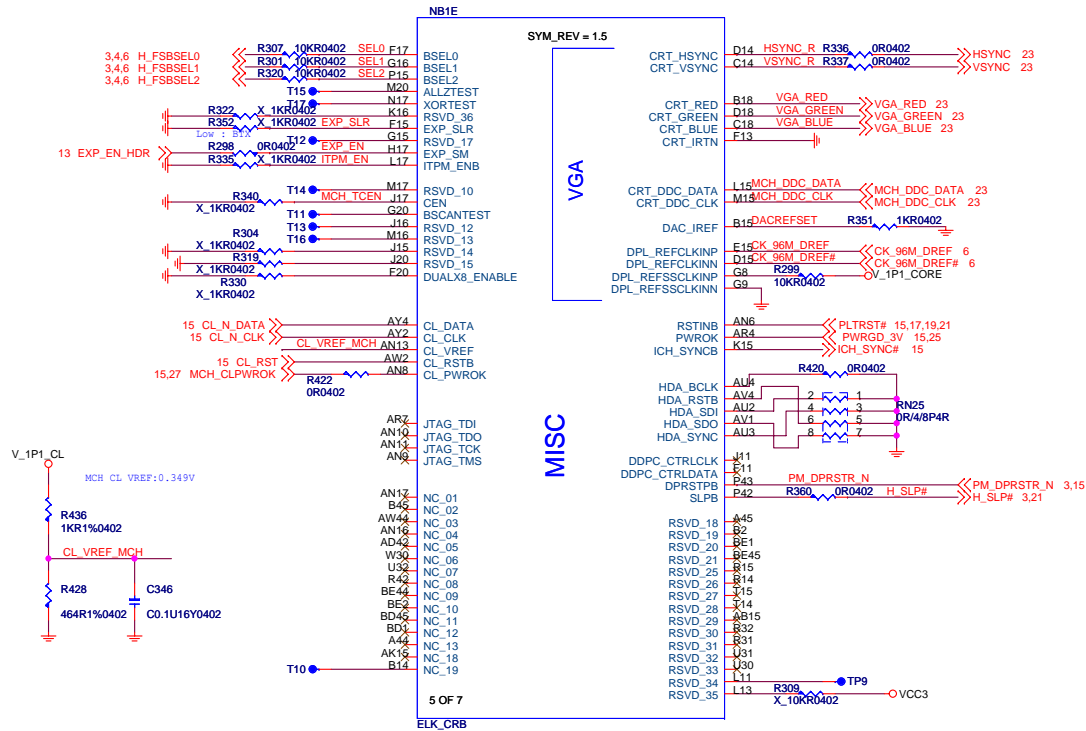




VDD_CK Decoupling

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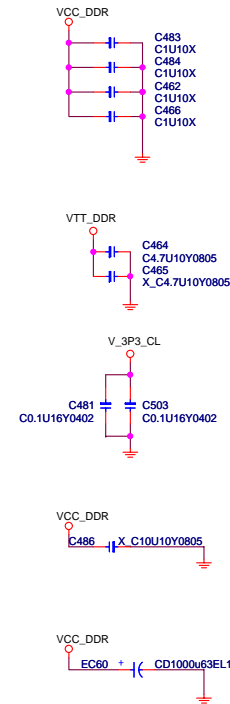
ITPM_ENB
 Integrated TPM Enable:
 0=Enable iTPM
 1=Disable iTPM

DualX8_Enable
 0=2X8 PCIe Ports Enable
 1=1X16 PCIe Port Enable

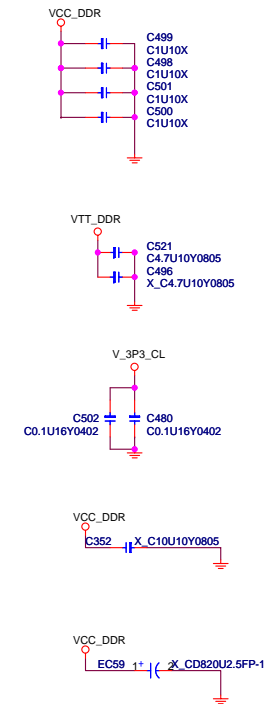
Primary_PEG_Presence
 DEMO BOARD CHANGE
 Primary PCIe port Detect:
 0=PCIe Card is in Primary Slot
 1=PCIe Card is not in Primary Slot

PIN	H	L	Description
EXP_SLR	Normal	Reverse	PCI_E Lane Reversal
EXP_EN	Concurrent	Non-concurrent	PCI_E/SUDVO co-existence
MCH_TCEN	Enable	Disable	PCI confidentiality

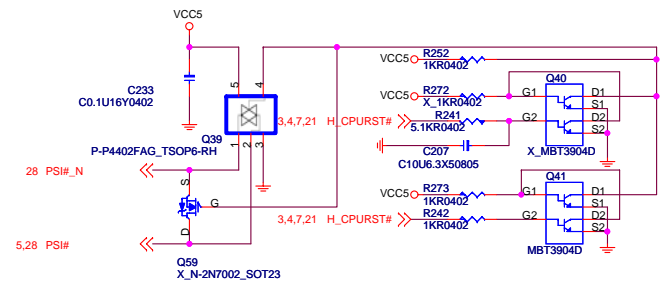
DIMM1 decoupling cap



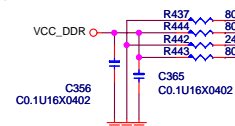
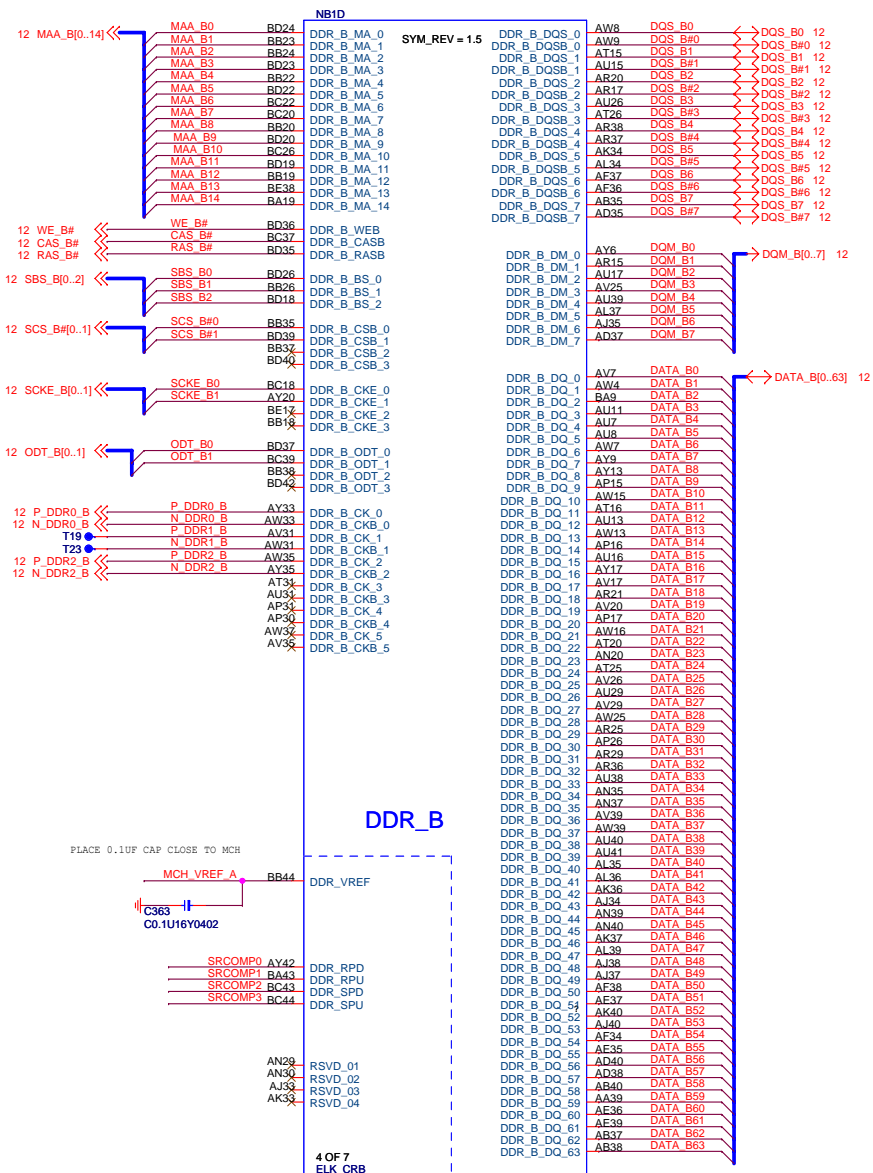
DIMM1 decoupling cap

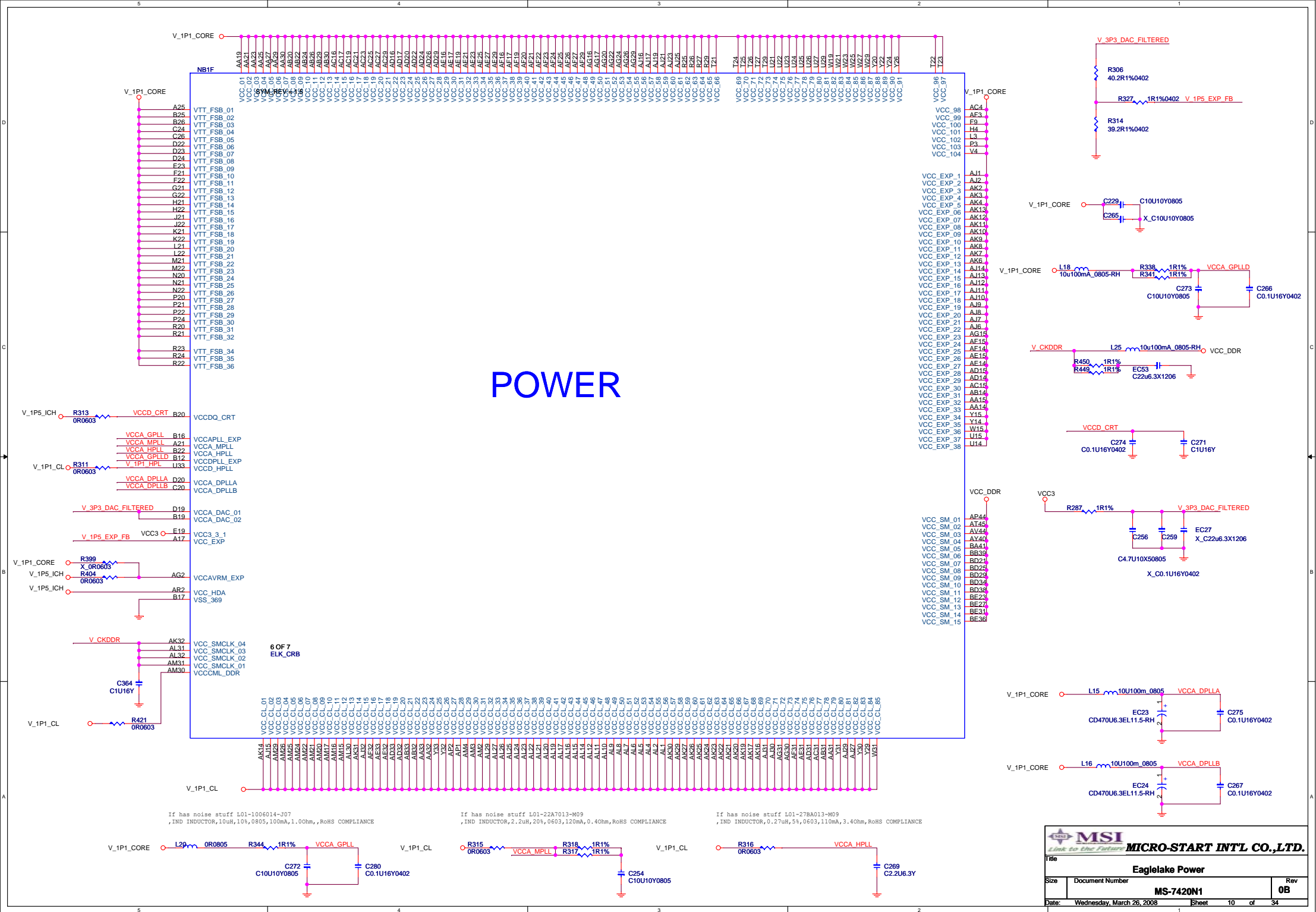


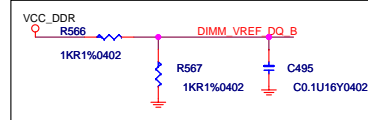
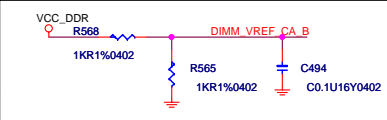
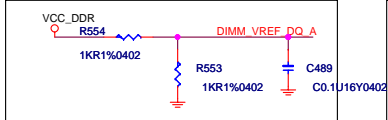
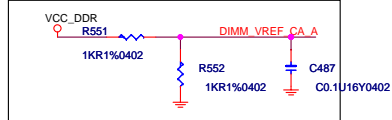
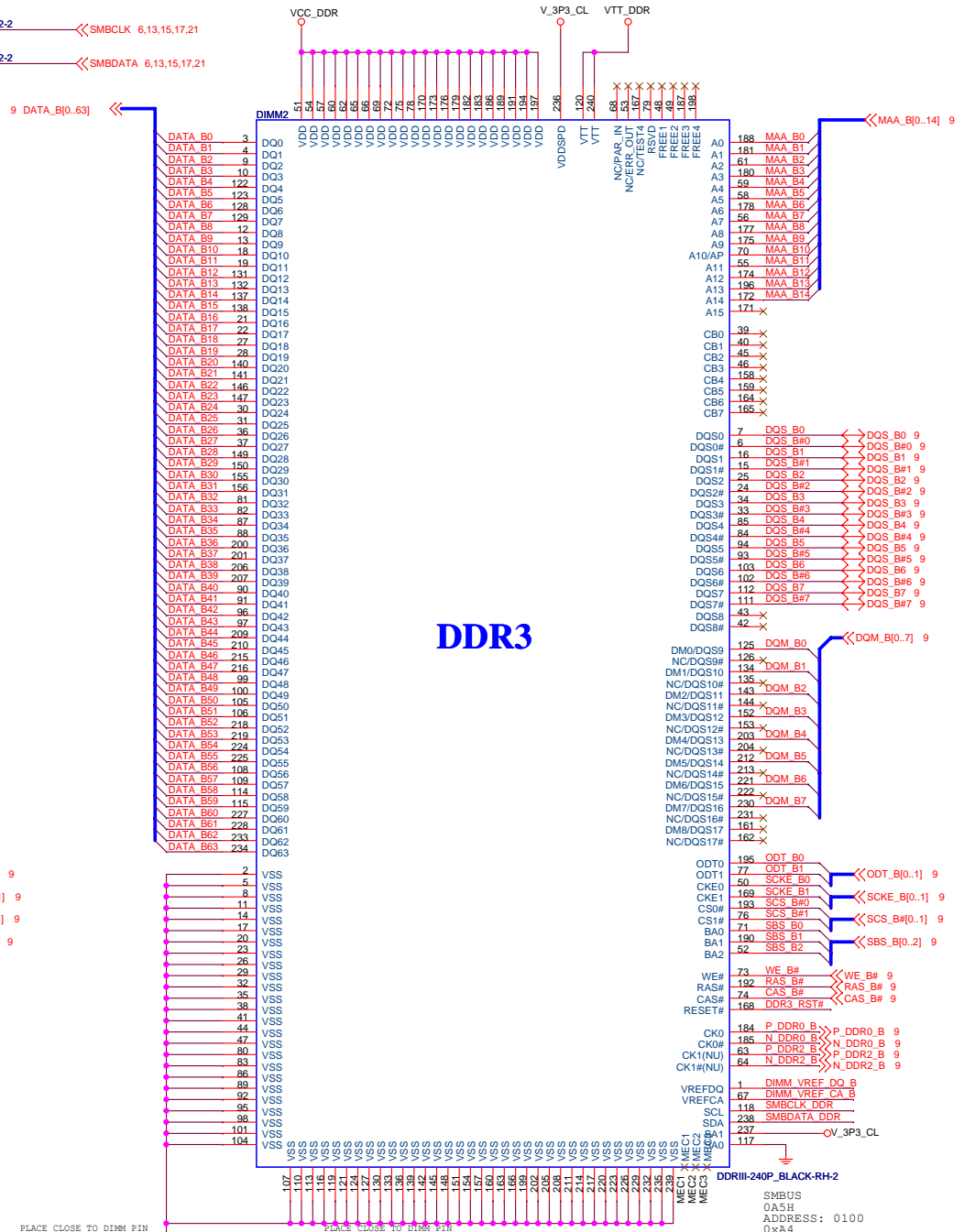
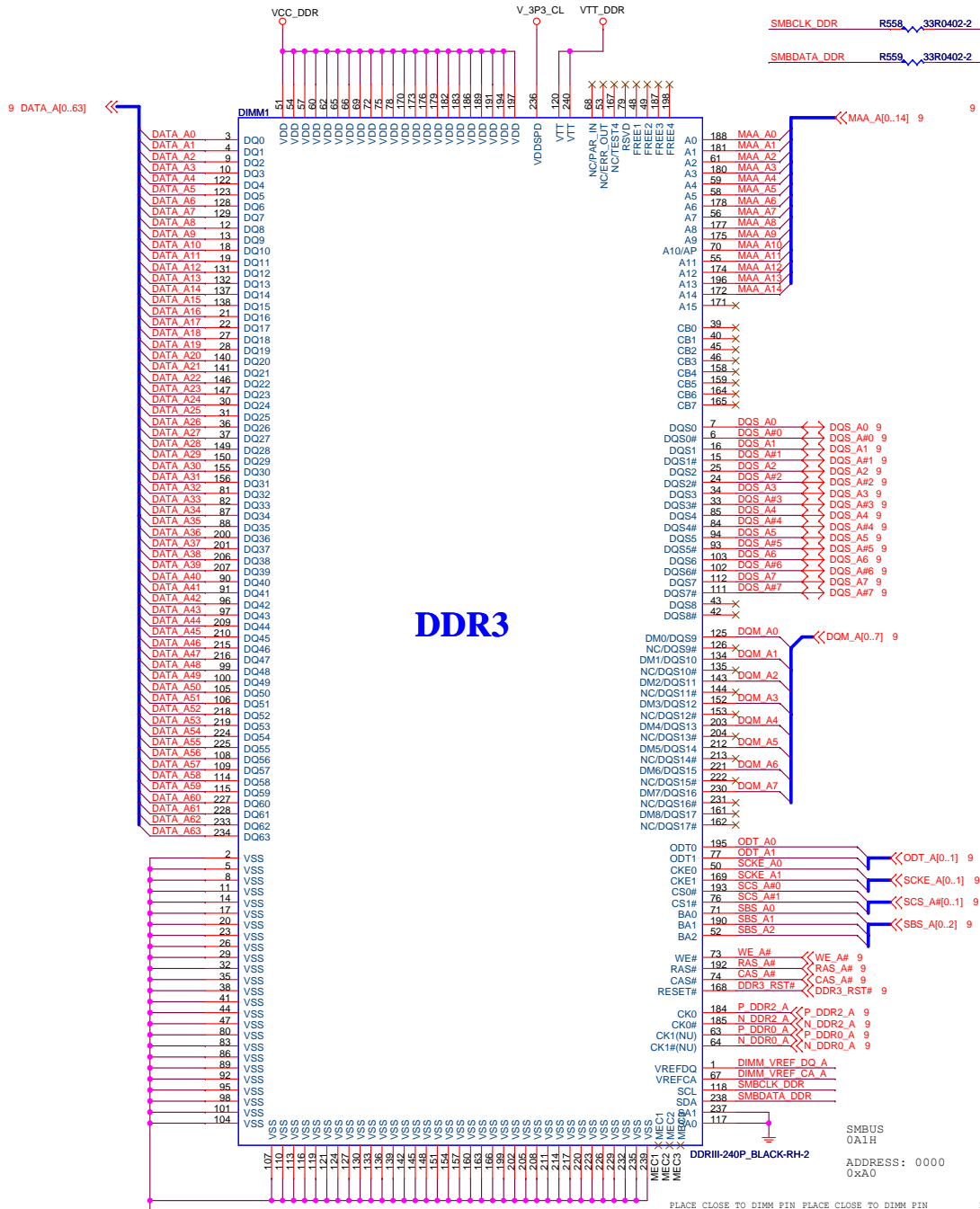
PSI(POWER STATE INDICATOR)

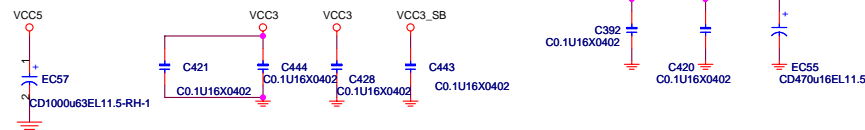


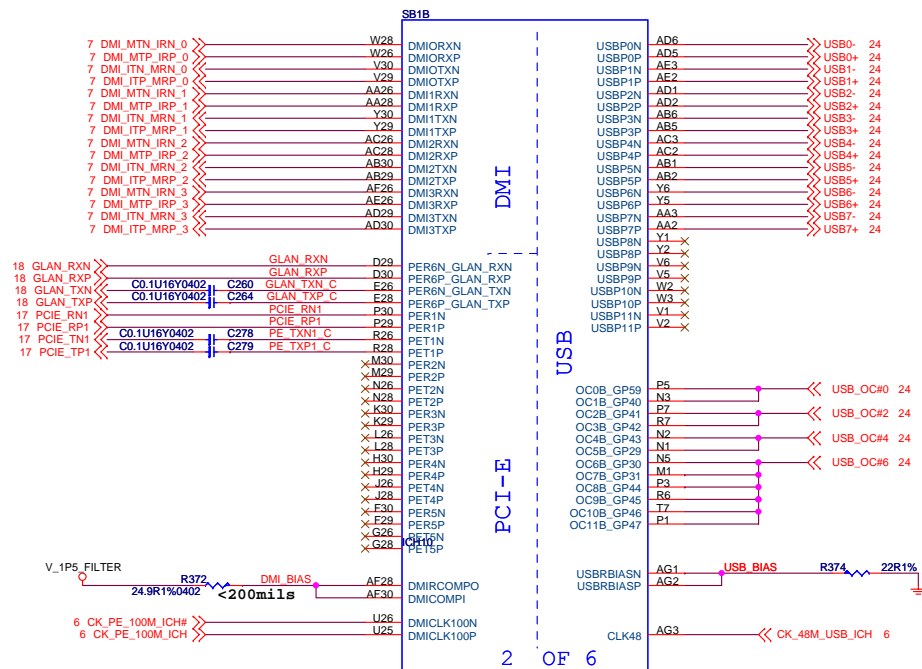
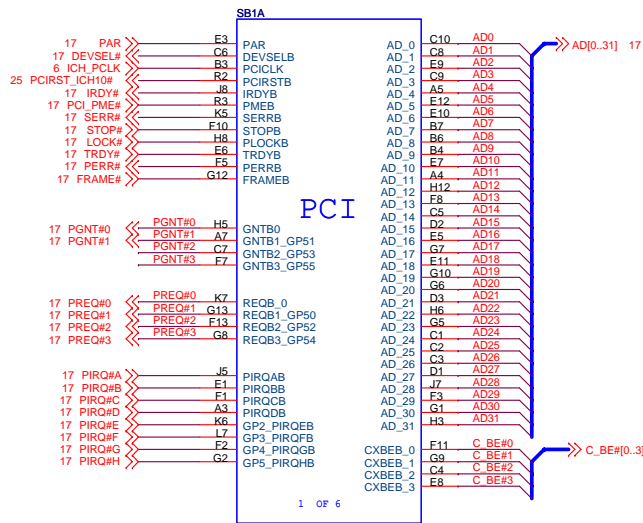
PDG:page 438 ,Please put near PWM



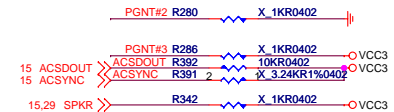




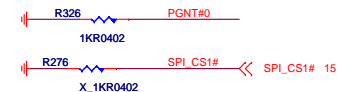




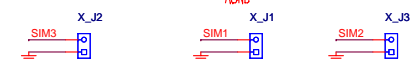
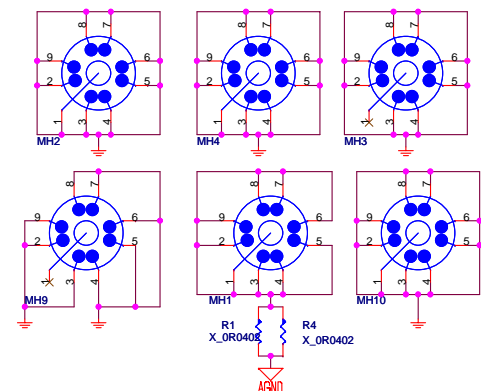
ICH10 H/W STRAPS			
SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERRIDE
INTVRMEN	EN	DIS	INT VRM
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	EN	DIS	Danbury Tec.
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)



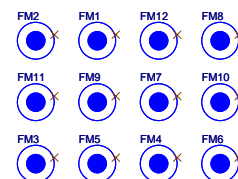
BOOT SELECT STRAPS			
BOOT DEVICE	GNT#0	SPI_CS1#	
FWH	1	1	
SPI	0	X	(Default)
PCI	1	0	



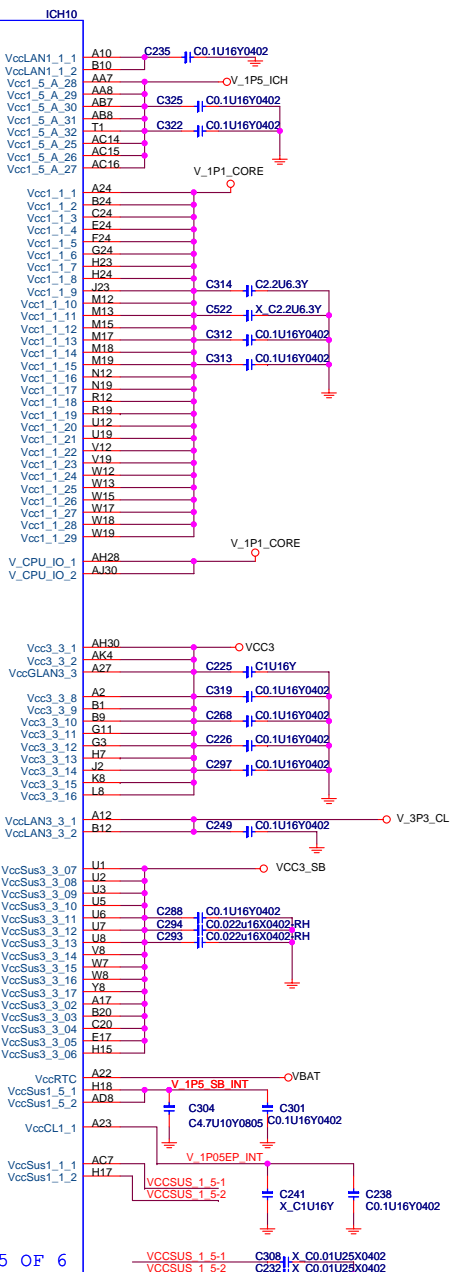
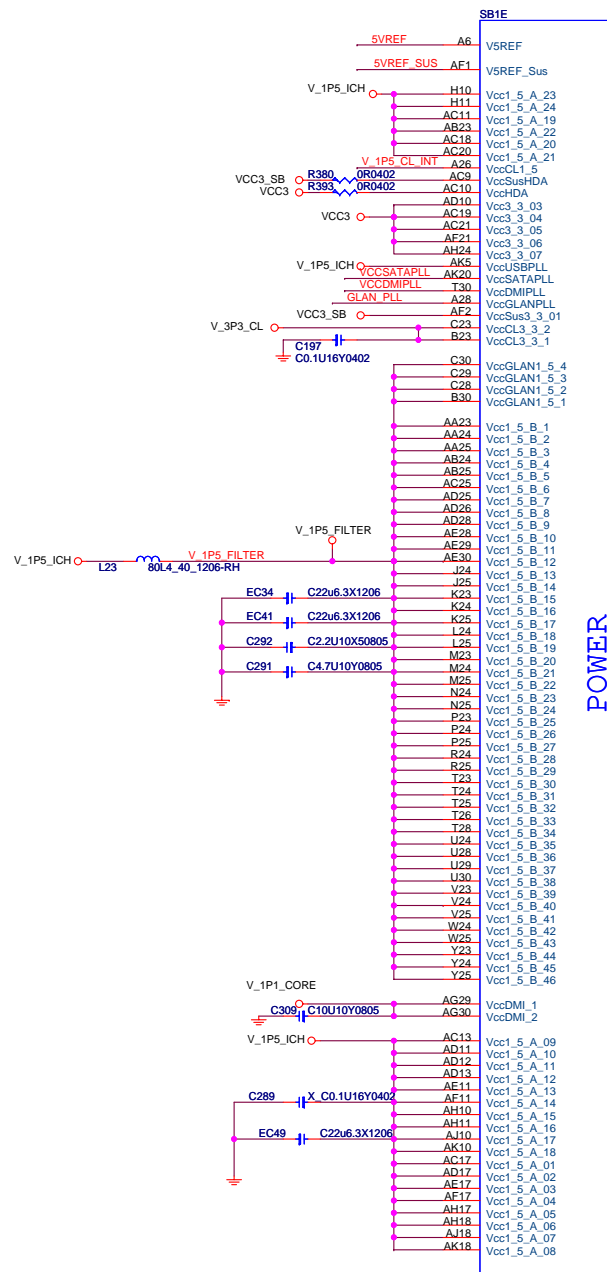
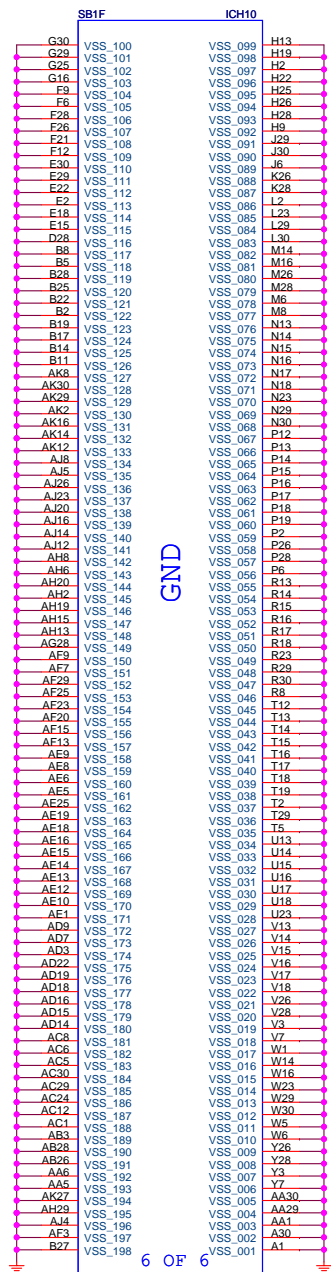
Mounting Holes



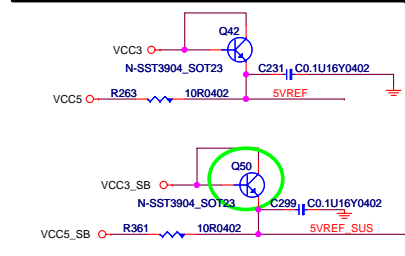
Optics Orientation Holes



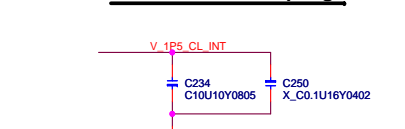
MICRO-START INT'L CO.,LTD.			
Title INTEL ICH10 PART1			
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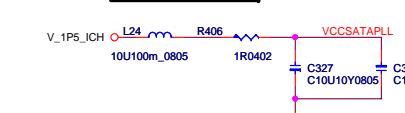
5VREF & 5VREF_SUS Sequencing Circuit



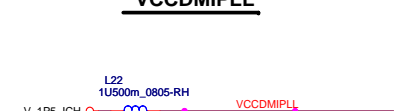
V_1P5_CL decoupling



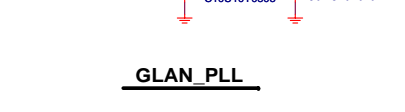
VCCSATAPLL



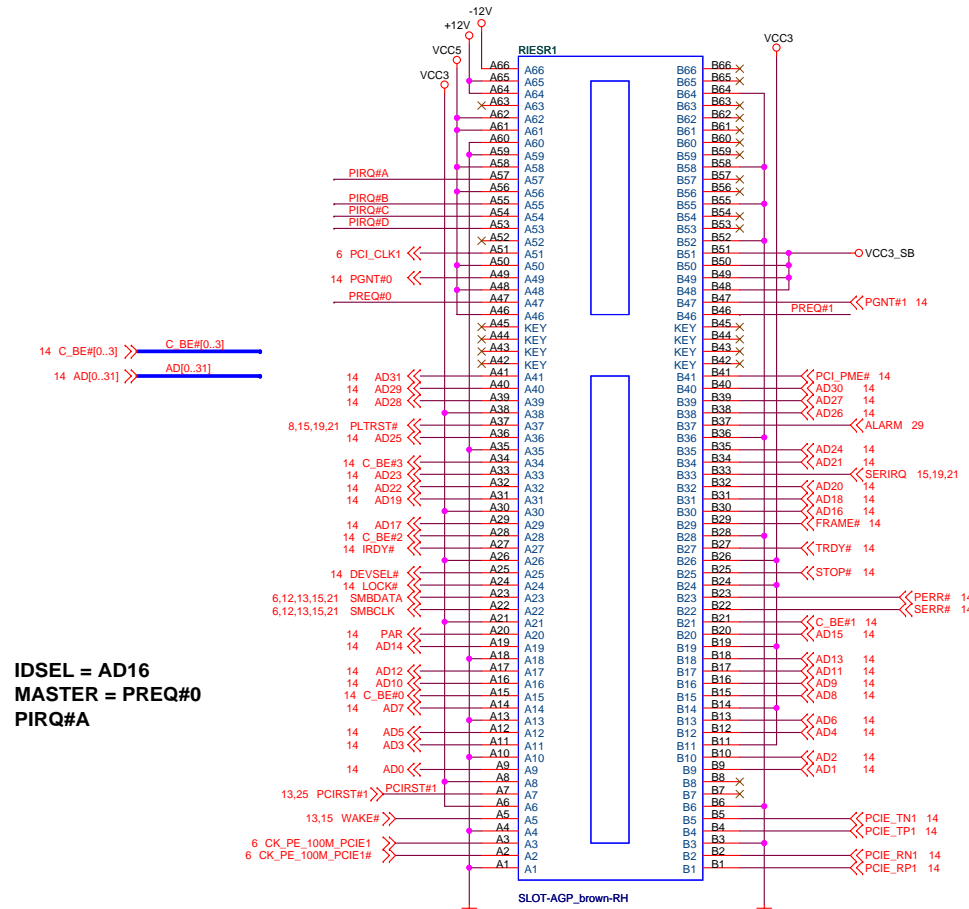
VCCDMIPLL



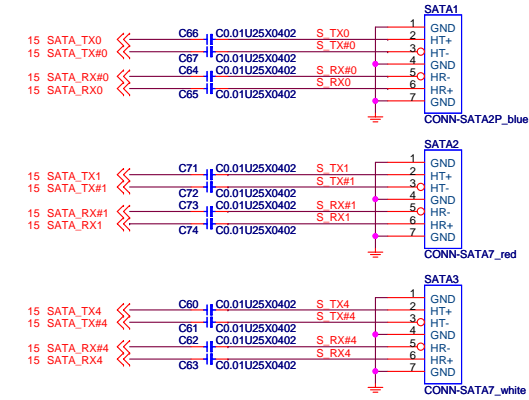
GLAN_PLL



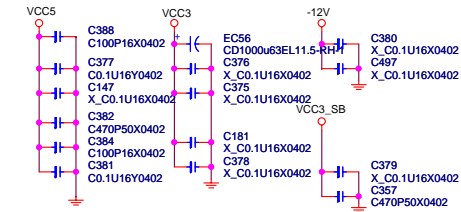
LE riser card interface



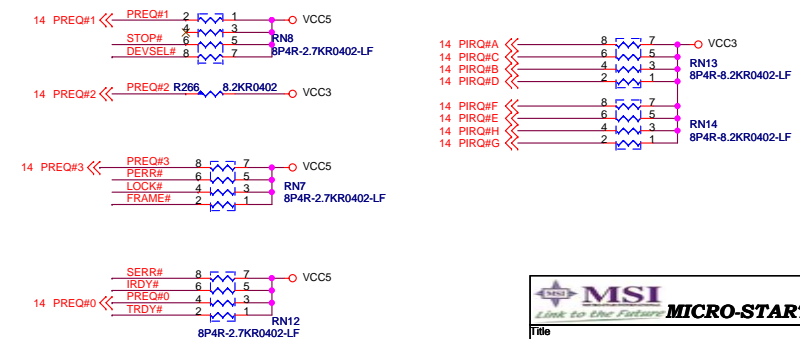
SERIAL ATA CONNECTOR BLOCK



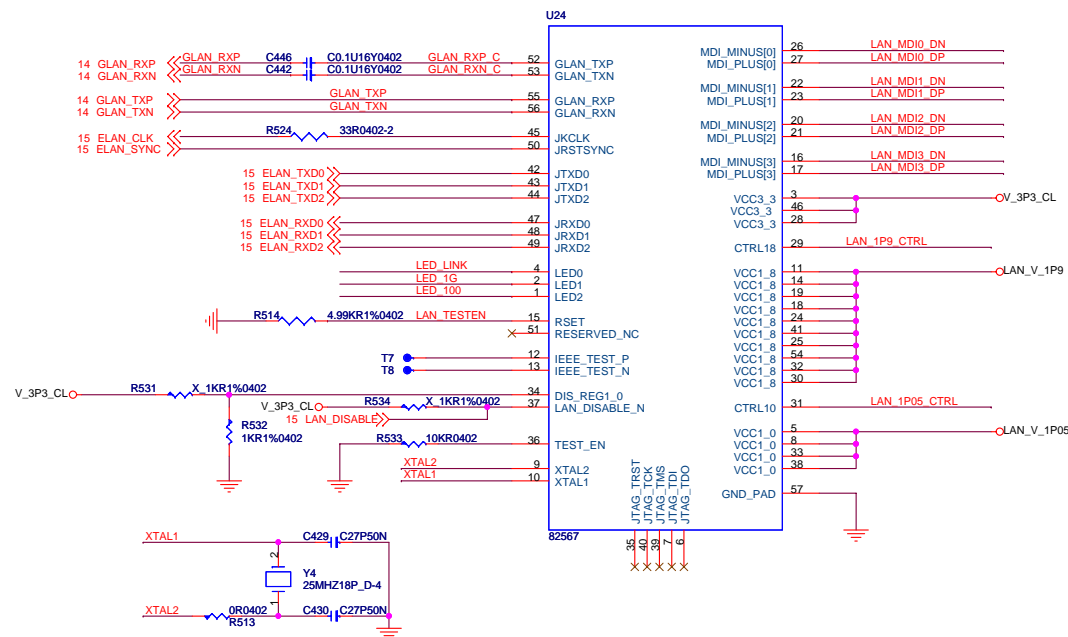
PCI SLOT DECOUPLING CAPACITORS



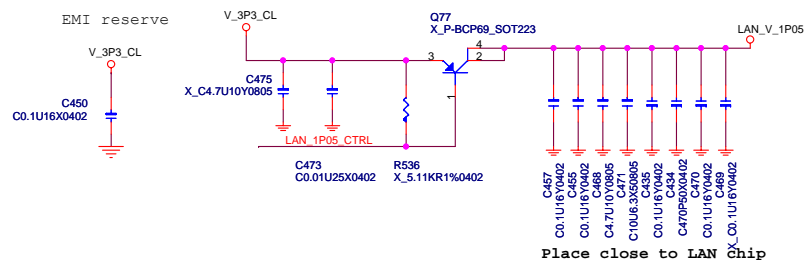
PCI PULL-UP / DOWN RESISTORS



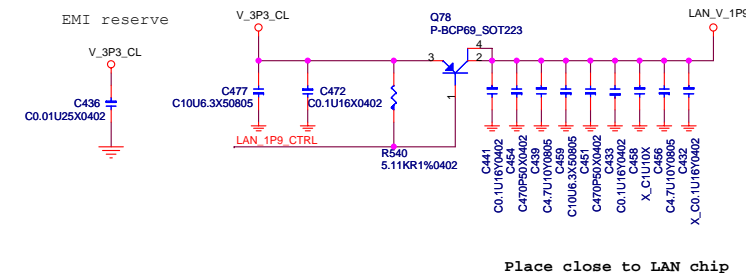
INTEL 82567(Boanman)



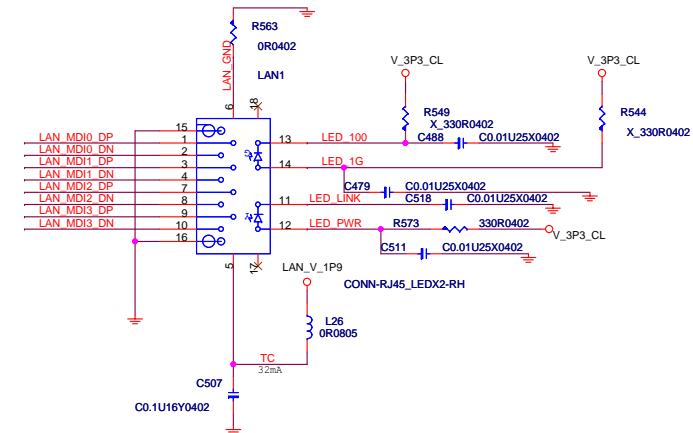
LAN 1P0 POWER (277.2mA)



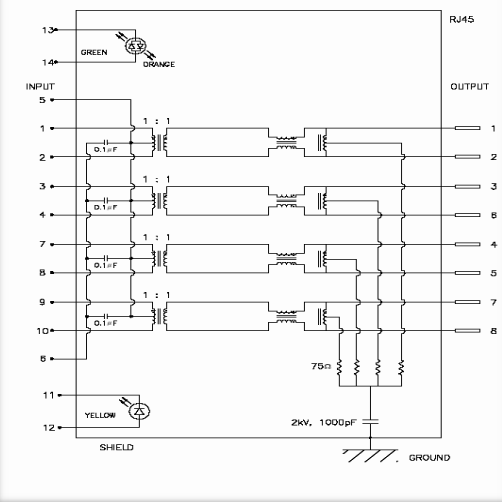
LAN 1P8 POWER (418.2mA)



LAN CONNECTOR

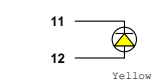
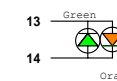


LAN1 structure

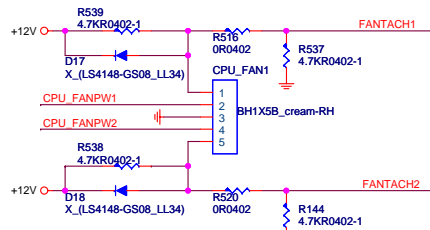


Speed LED Type
100Mbps : Orange
10Mbps : Green
10Mbps : LED off

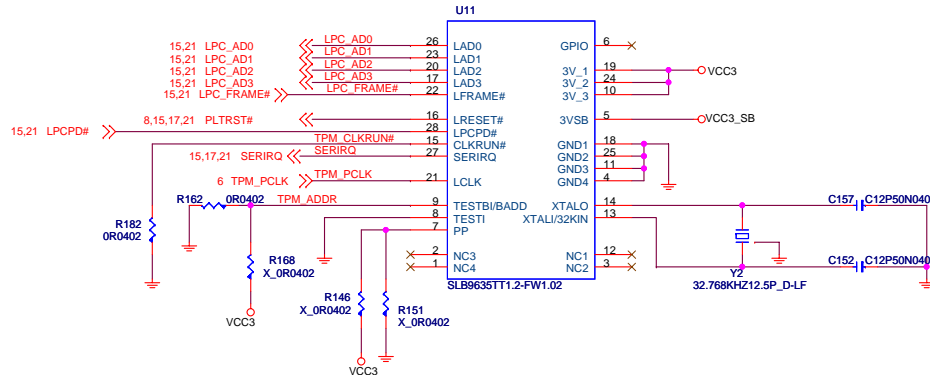
For Active/Link:
Yellow



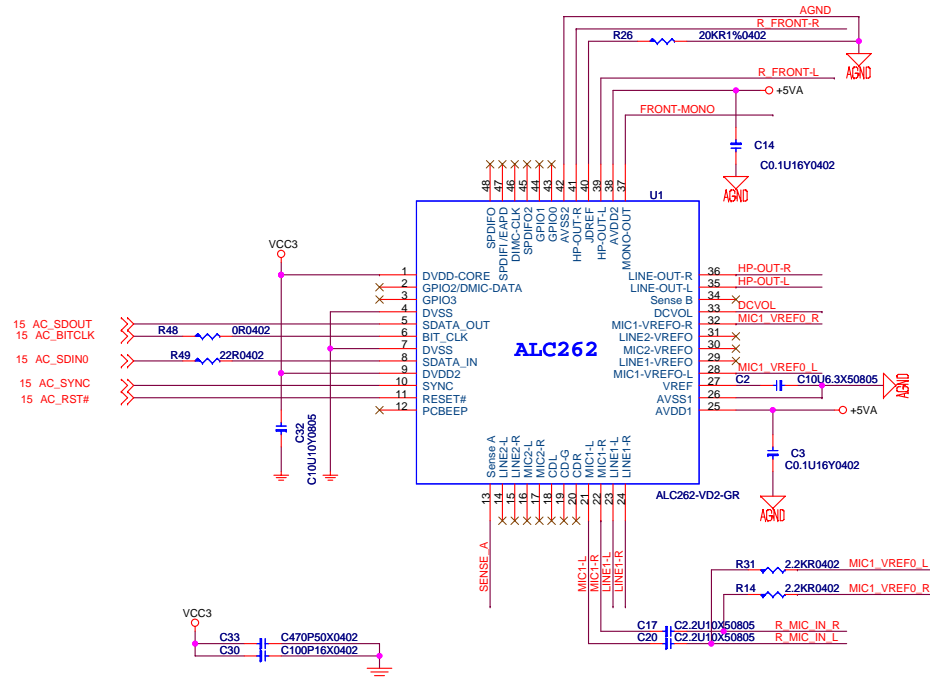
CPU FAN2



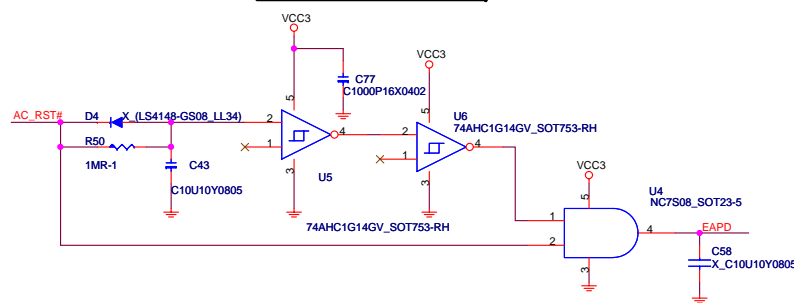
TPM 1.2



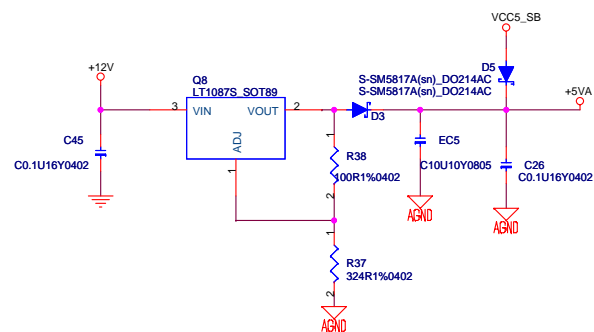
RELTEK HD ALC262VD2



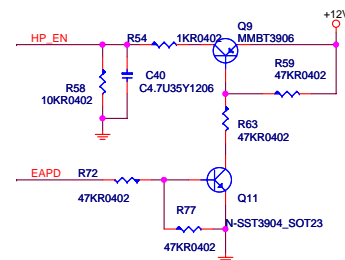
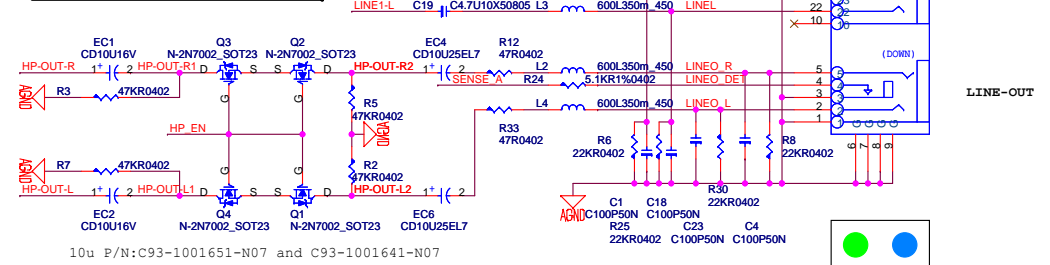
POP noise circuit



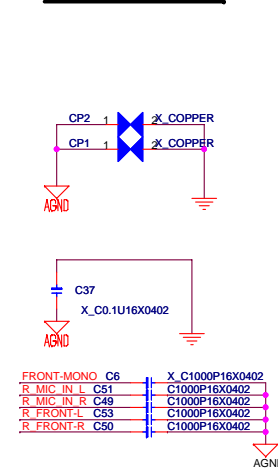
Audio CODEC REGULATOR



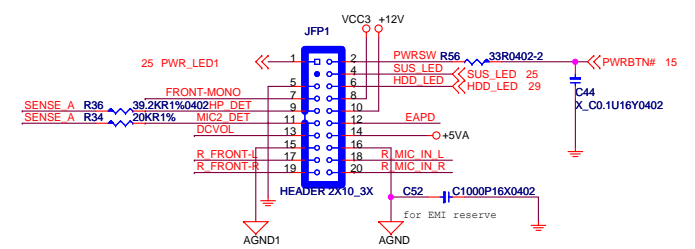
Smooth POP noise circuit



For EMI reserve

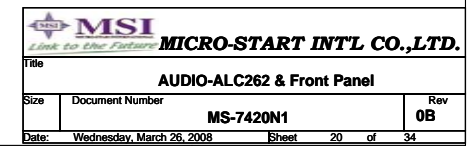
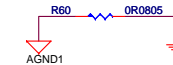


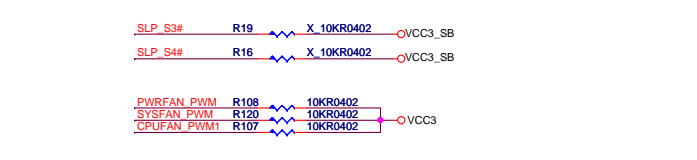
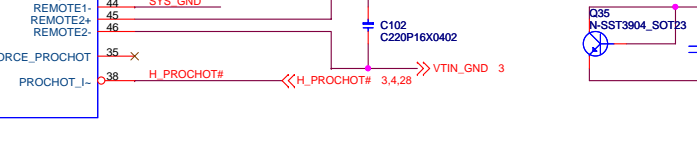
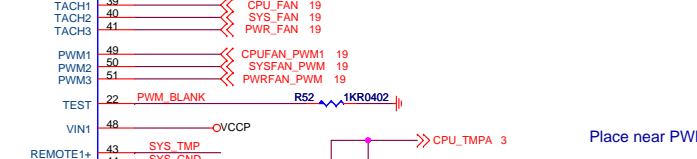
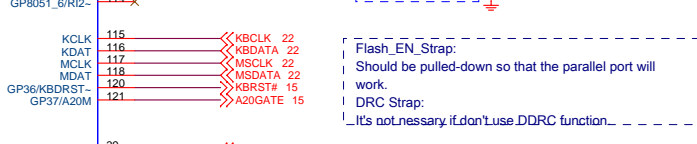
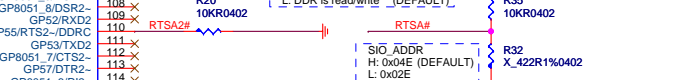
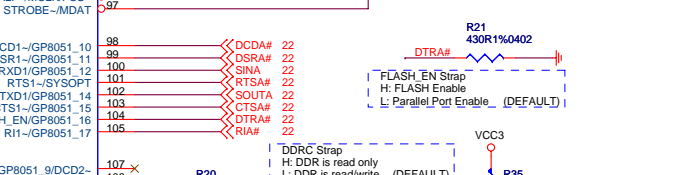
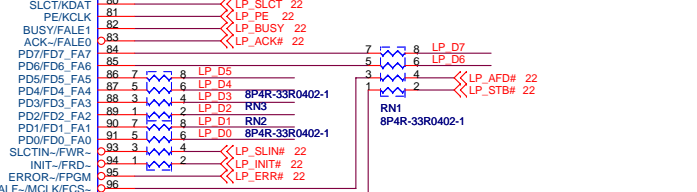
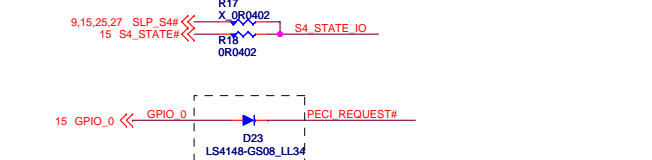
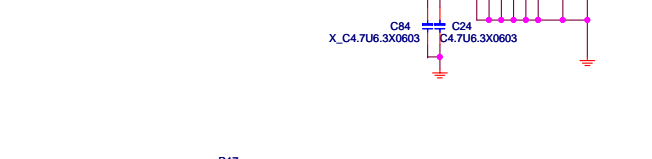
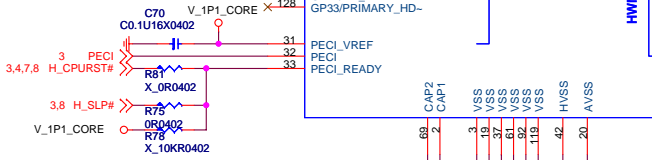
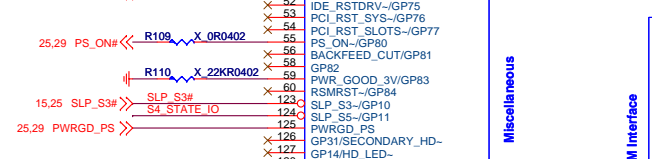
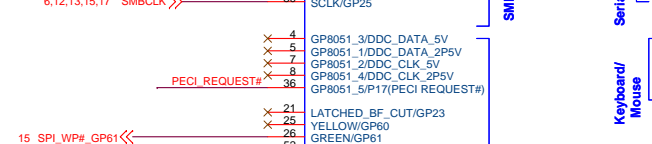
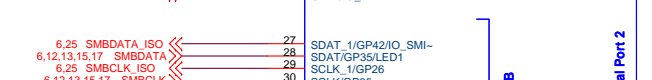
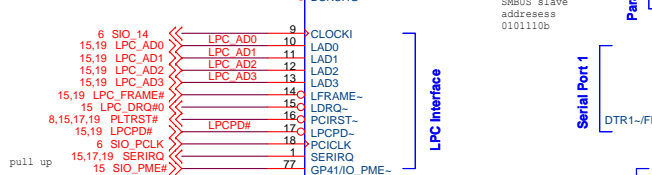
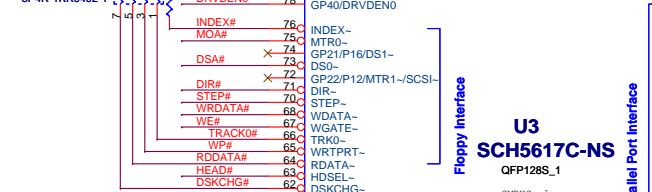
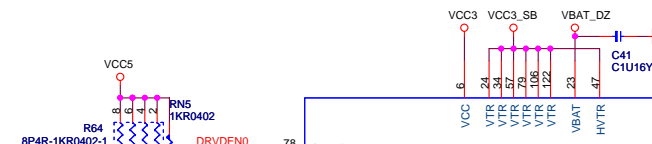
For Front Panel



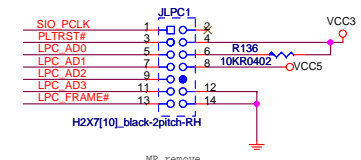
JFP1

1	<i>PWR_LED</i>	<i>POW_SW</i>
3	<i>NC</i>	<i>SLP_LED</i>
5	<i>GND</i>	<i>HDD_LED</i>
7	<i>Mono</i>	<i>VCC3</i>
9	<i>HP_DET</i>	<i>+12V</i>
11	<i>MIC_DET</i>	<i>EAPD</i>
13	<i>DCVOL</i>	<i>+5VA</i>
15	<i>AGND1</i>	<i>AGND</i>
17	<i>FRONT_L</i>	<i>MIC_L</i>
19	<i>FRONT_R</i>	<i>MIC_R</i>

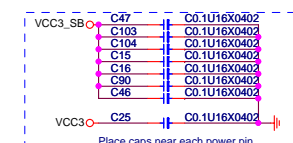




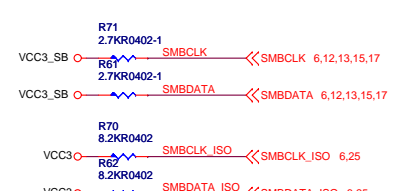
Debug port



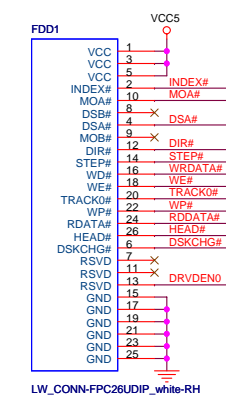
SIO power decoupling




SMBUS pull-up resistor

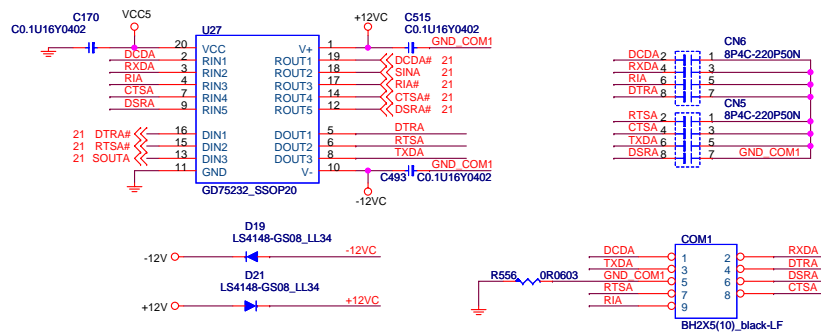


1/2" Notebook type

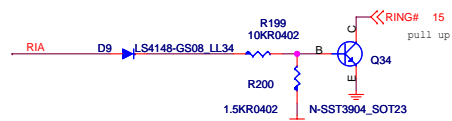


			
Link to the Future			
MICRO-START INTL CO.,LTD.			
Title			
SIO SMSC SCH5017 & FDD			
Size	Document Number	Rev	
	MS-7420N1	0B	
Date:	Wednesday, March 26, 2008	Sheet	21 of 34

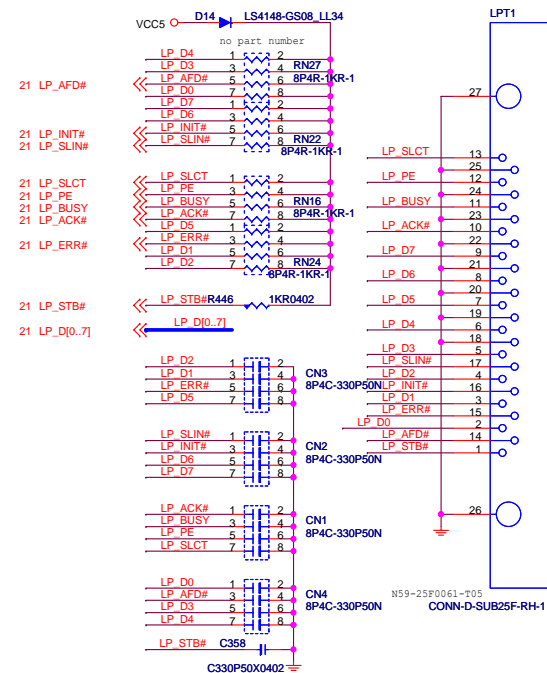
SERIAL PORT 1



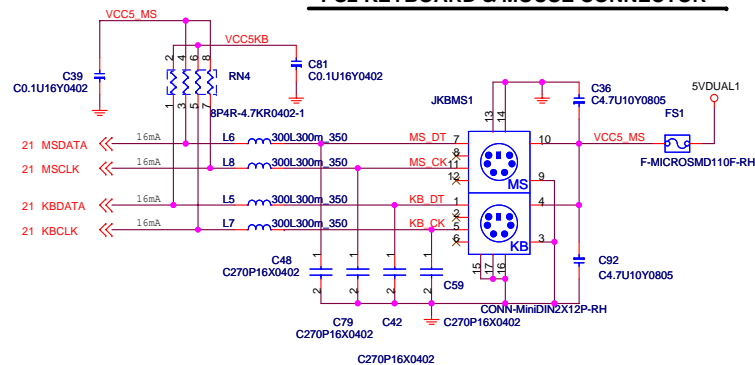
Wake On Modem Header



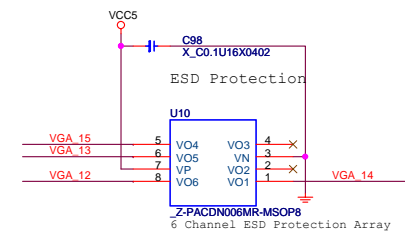
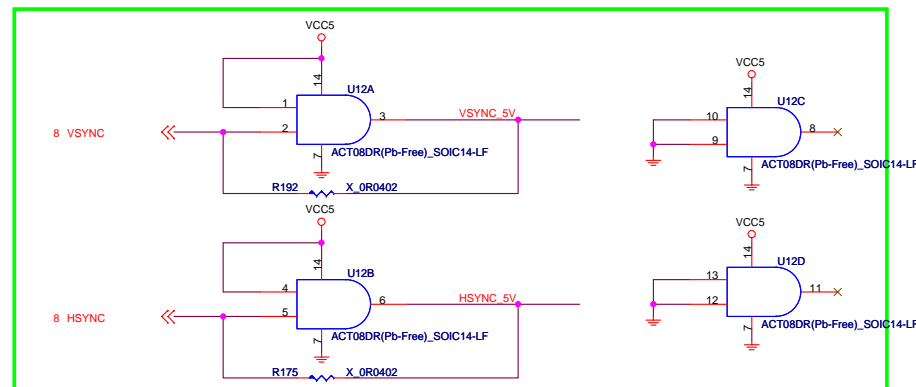
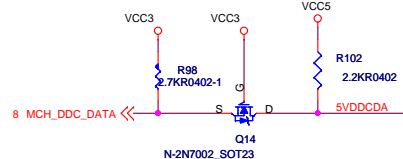
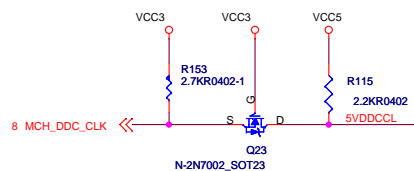
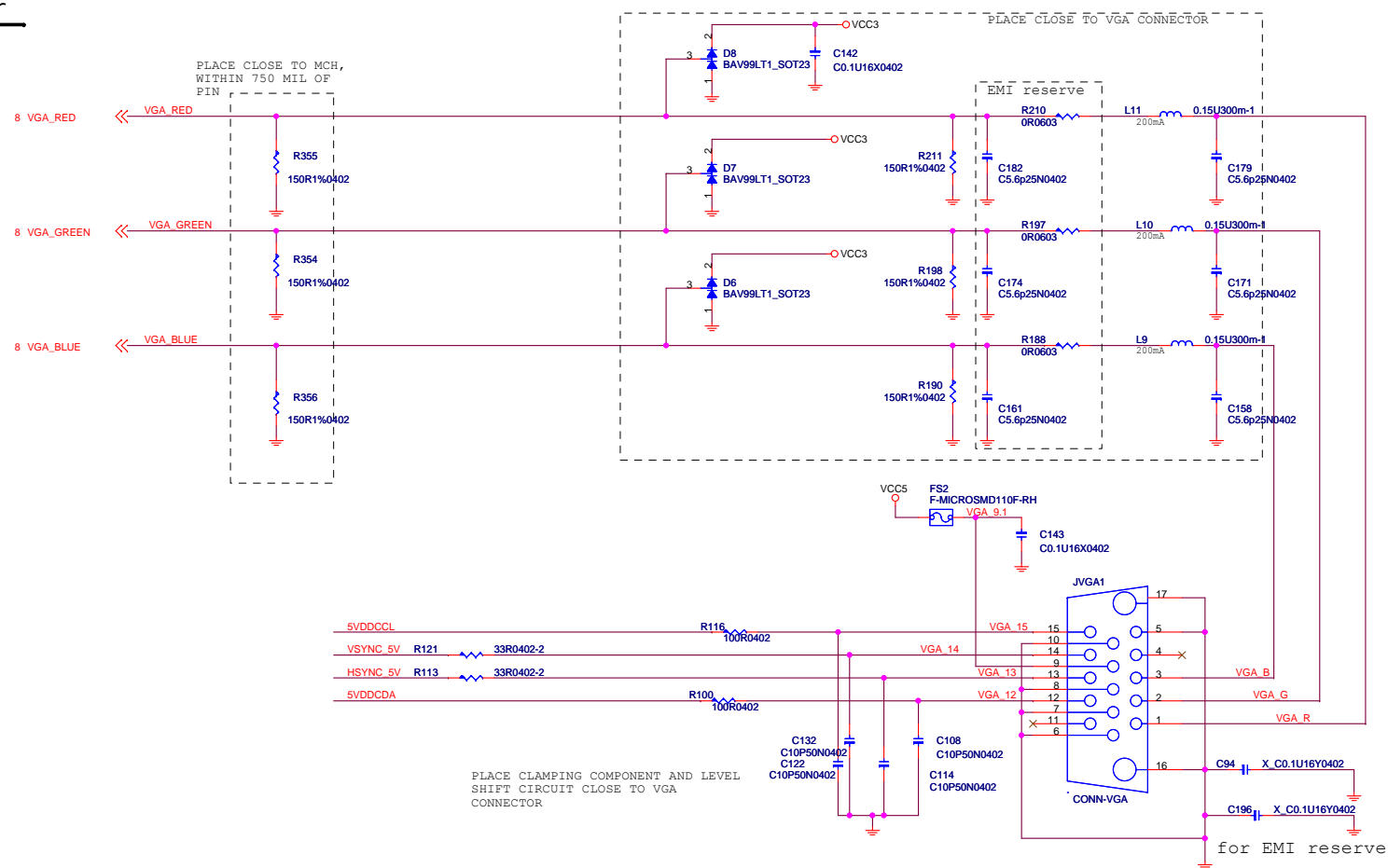
PARALLAL PORT



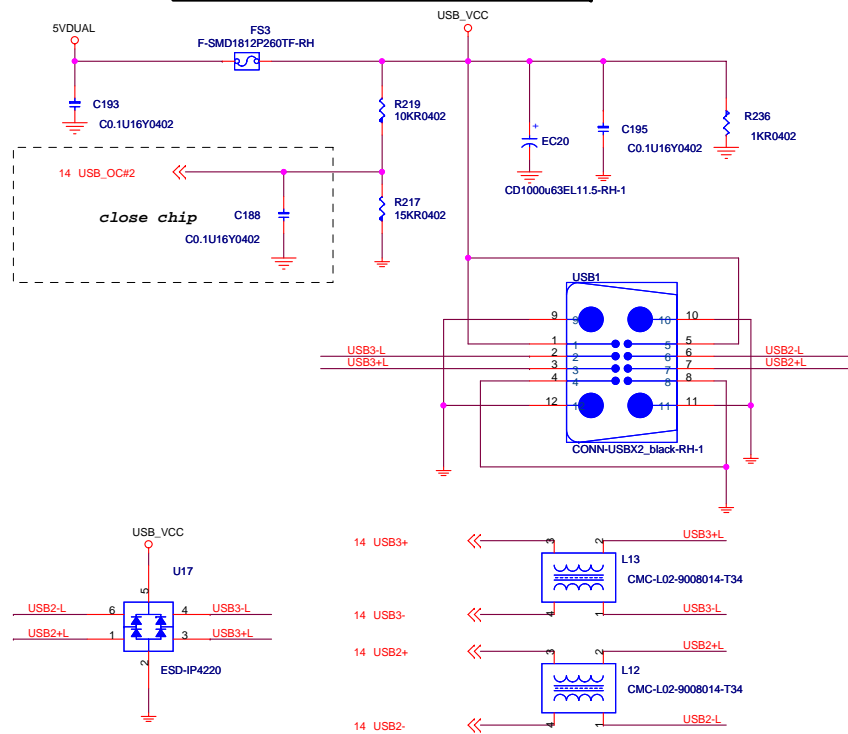
PS2 KEYBOARD & MOUSE CONNECTOR



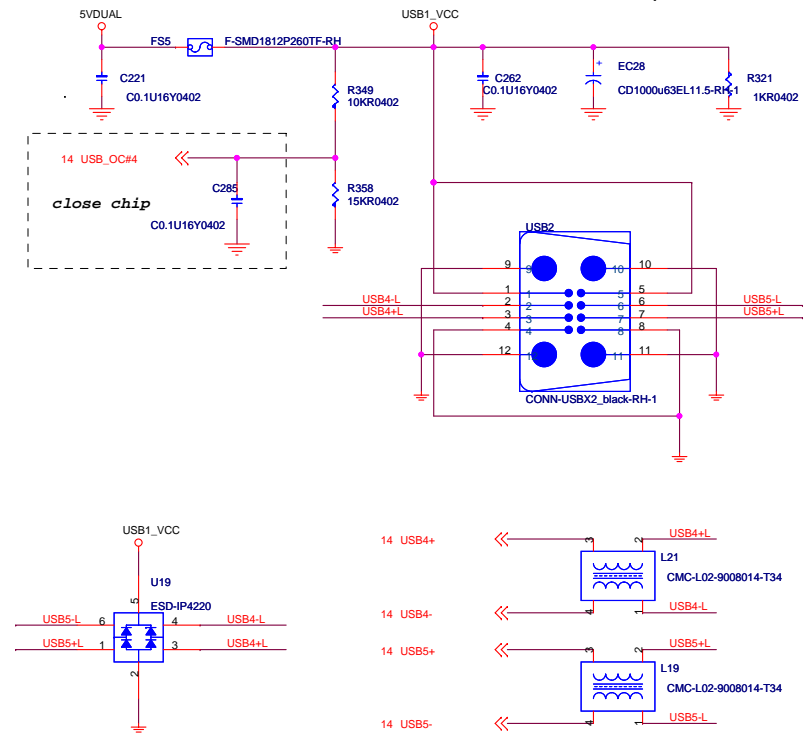
Video Connector



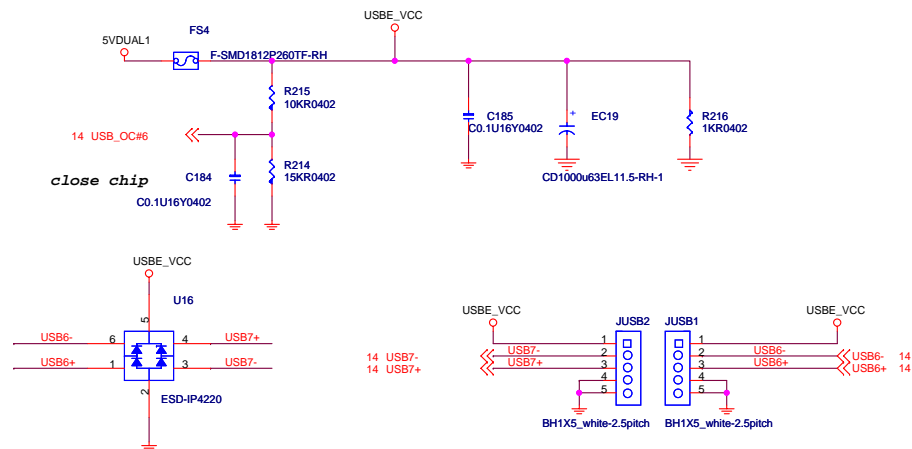
REAR PANEL USB PORT 2,3 CONNECTOR



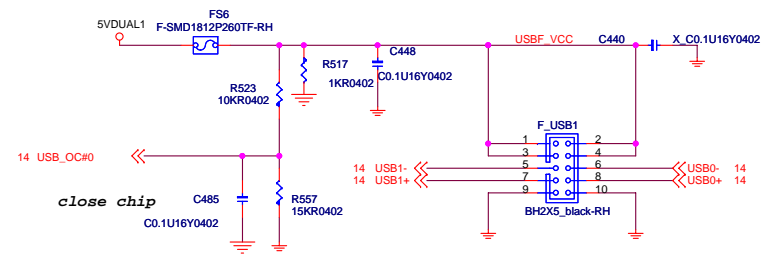
REAR PANEL USB PORT 4,5 CONNECTOR



RESERVE EXTERNAL USB PORT 6,7



FRONT PANEL USB PORT 0,1 CONNECTOR



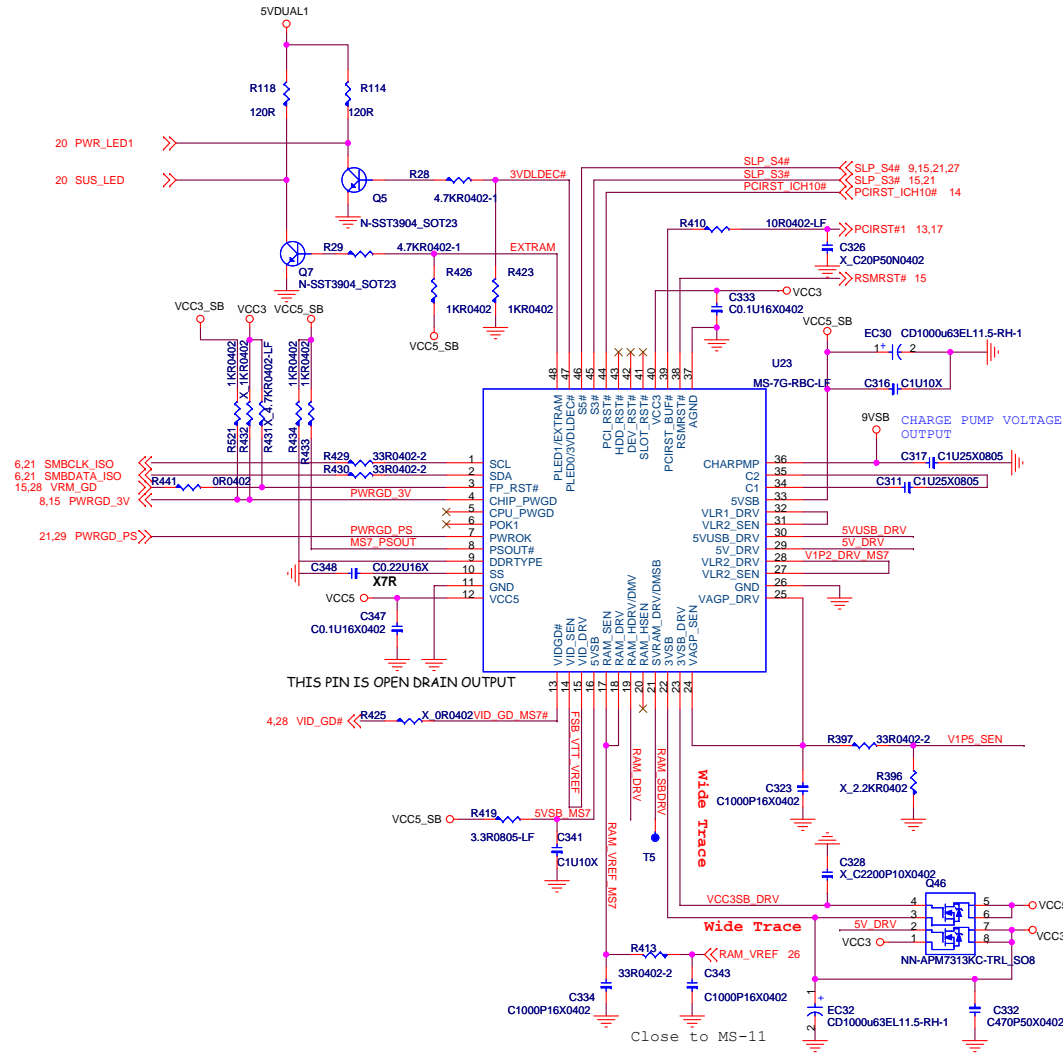
ACPI Controller

VDIMM LINEAR OR PWM SELECT

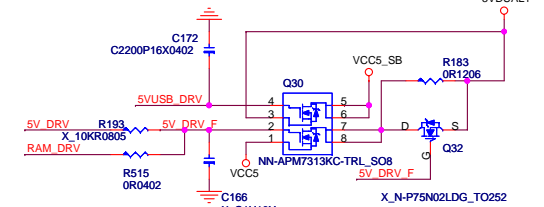
VDIMM MODE EXTRAM
 LINEAR REGULATOR PULL LOW
 PWM REGULATOR PULL HIGH

3VSB MODE SELECT

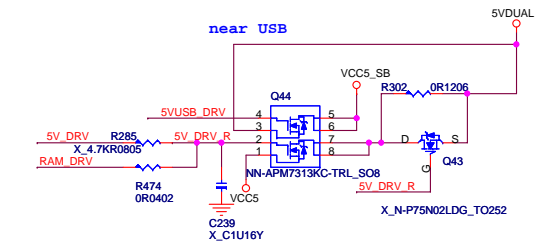
3VSB MODE BVDLDEC#
 SINGLE MOSFET PULL HIGH
 DUAL MOSFET PULL LOW



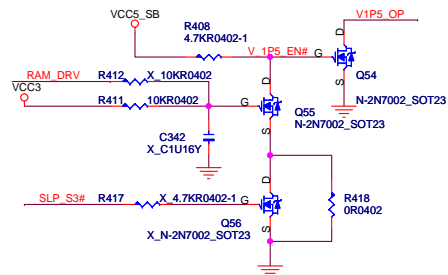
5V DUAL Front Power (2A)



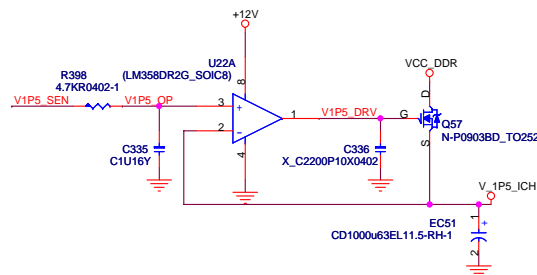
5V DUAL Rear Power (2A)



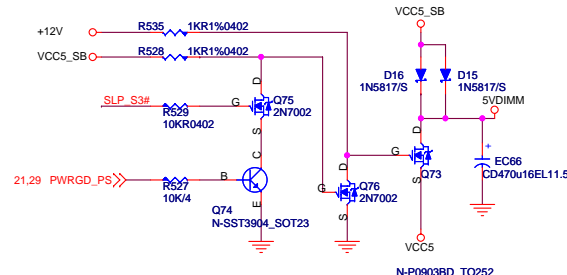
V1P5_SEN S3 power sequency



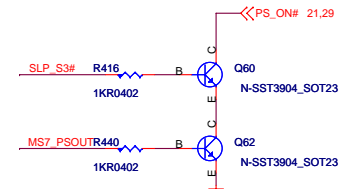
ICH10 1.5V POWER (2.385A)



5VDIMM



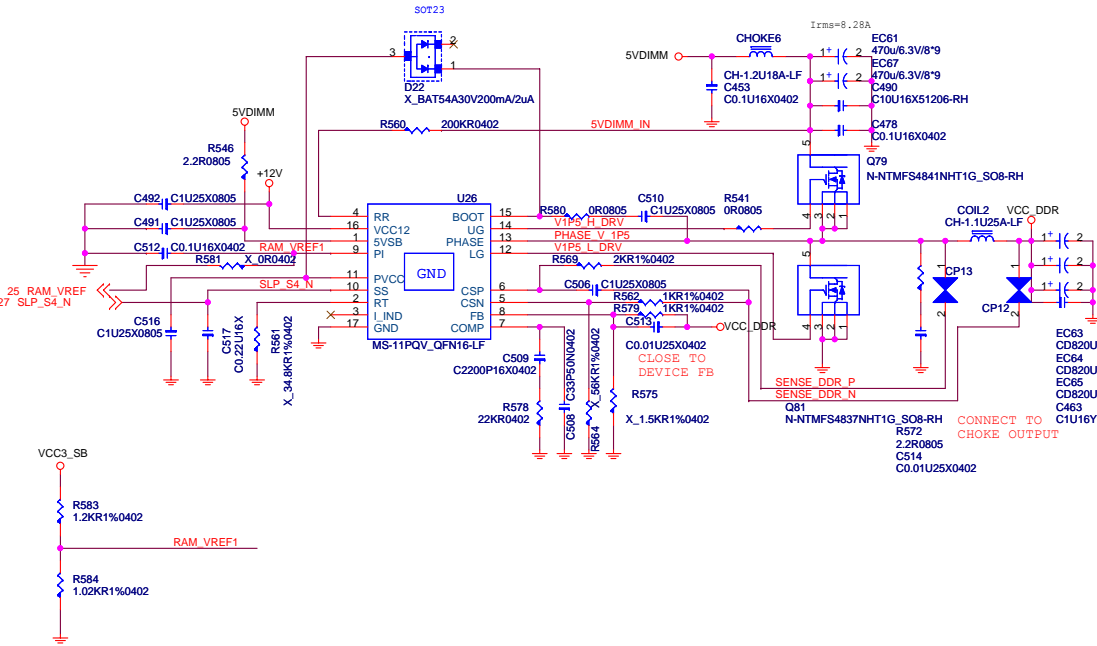
PSON#



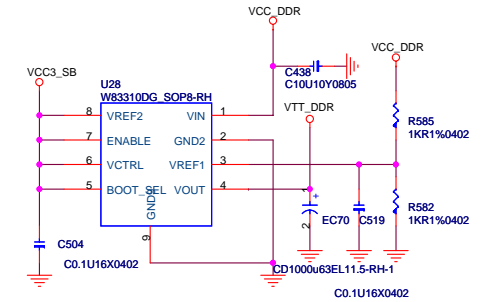
MICRO-START INTL CO.,LTD.

ACPI CONTROLLER MS7		
Size	Document Number	Rev
	MS-7420N1	0B
Date:	Thursday, March 13, 2008	Sheet 25 of 34

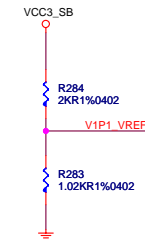
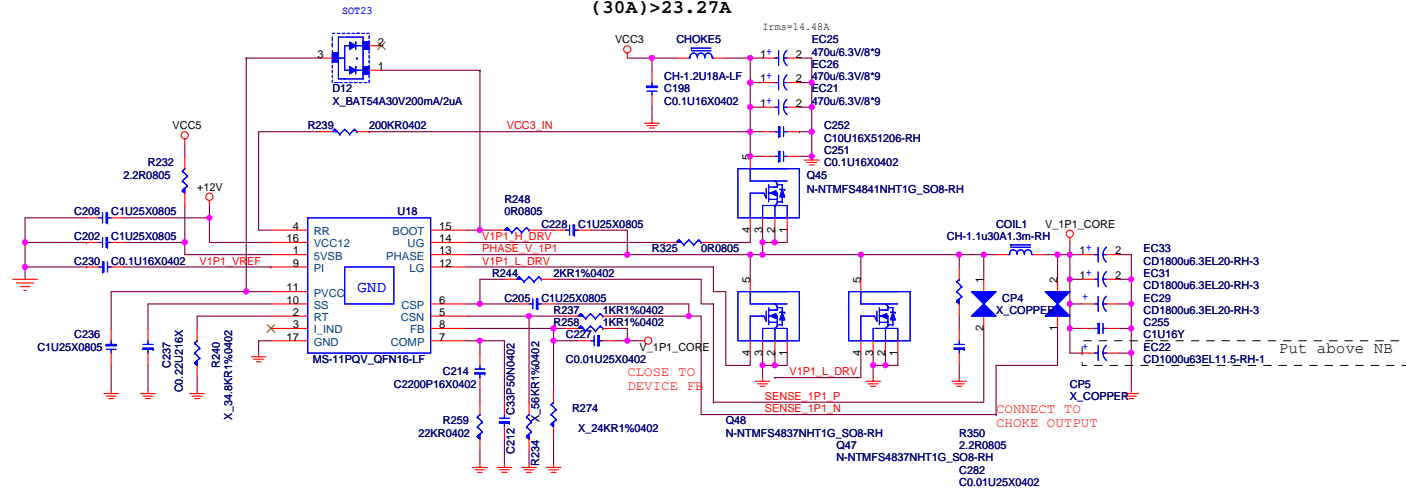
DDRIII 1.5V POWER (18A) > 13.86A

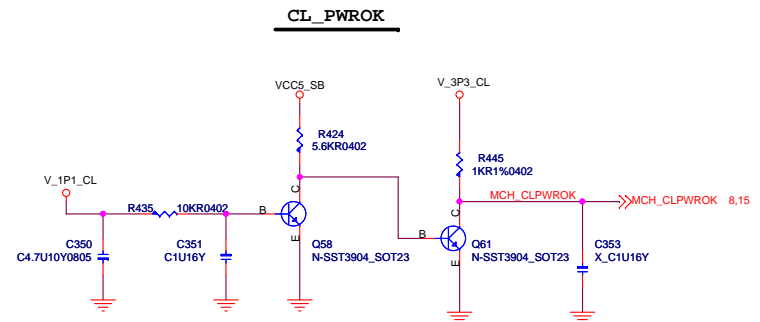
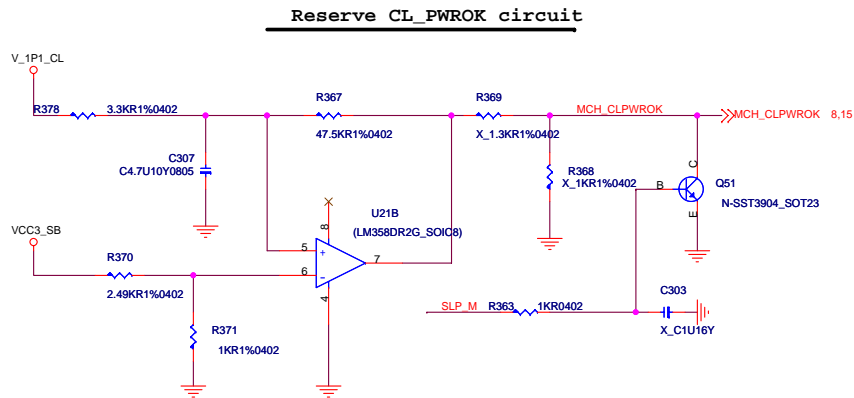
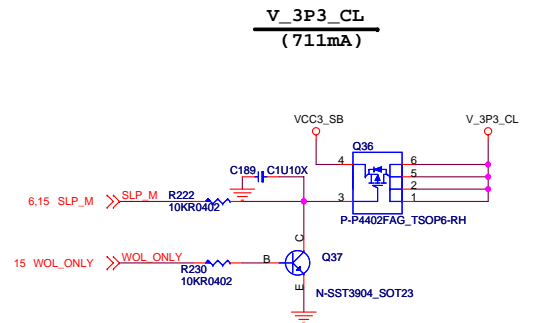
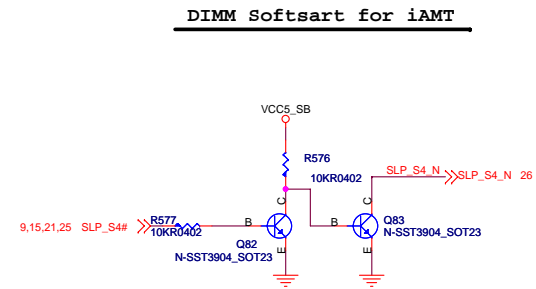
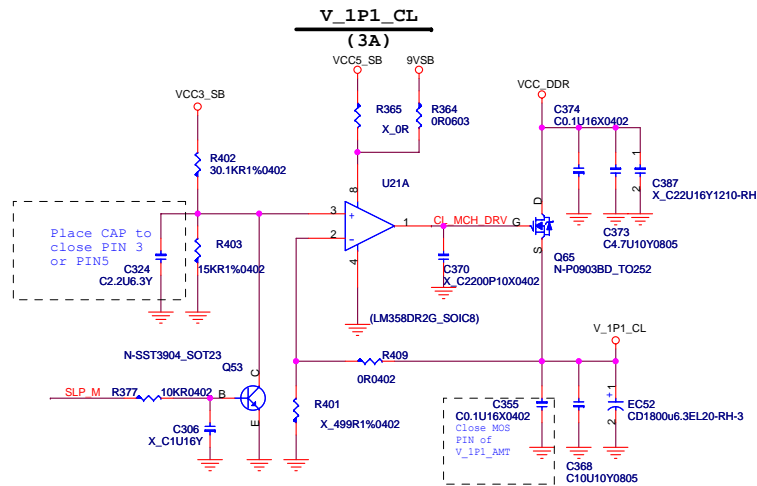


DDR VTT Power (0.83A)



GMCH/ICH10 1.1V POWER (30A) > 23.27A





Note:
 SLP_S4#
 AMT Disable-->indicate ACPI S4 state,DRAM power off.
 AMT Enable-->not be asserted ACPI S4 state,DRAM power ON
 SLP_M#
 AMT Enable SLP_M#-->Control the overall power to Intel AMT during ACPI S3-S5.
 S4_SATE#
 AMT Enable-->indication of ACPI S4 state

15 SATALED#

VCC5

R57 1KR0402

Q10

R55

22R0402

4.7KR0402-1 P-MMBT3906LT1G_SOT23-RH

R53

SATALED#

HDD_LED 20

$I_c=200mA$
 $V_{th}=5V$
 $V_{ds}=40V$

Remove after MP

H1X2_black-RH

R235

100R0402

FP_RST# 15

C206
C0.1U16Y0402

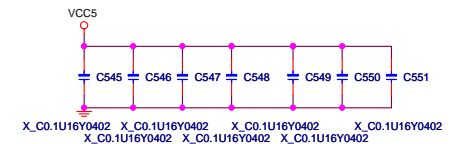
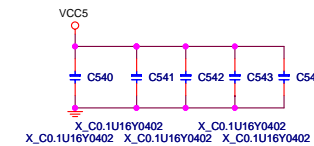
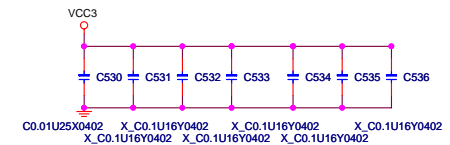
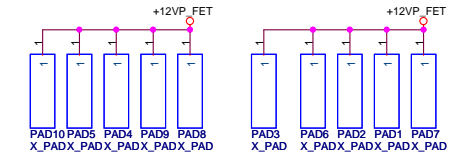
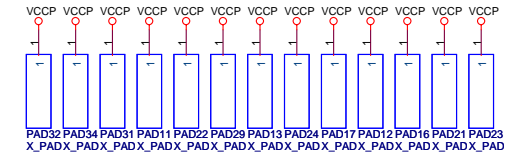
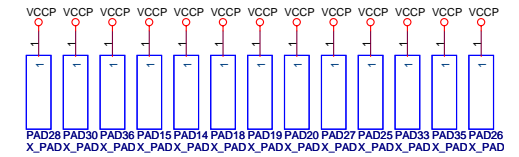
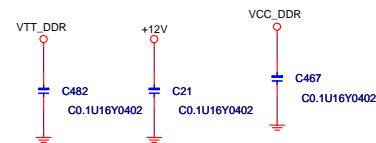
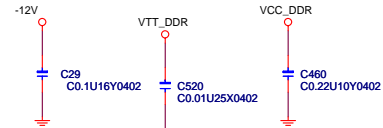
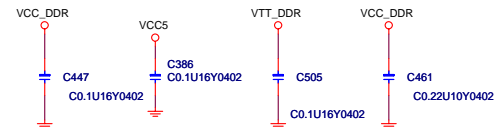
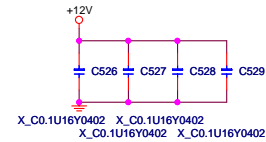
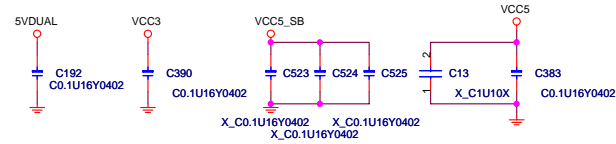
C201
X_C470P50X0402

The schematic diagram shows the connection of the alarm system components to the microcontroller pins. The buzzer (BZ1 BUZZER-LF) is connected to pin D13 (LS4148-GS08_LL34) and pin C4. The speaker (14,15 SPKR) is connected to pin R359 (2.7KR0402-1) and pin Q49 (N-SST3904_SOT23). The speaker is also connected to pin 17 (ALARM) and pin 8 (8P4R-470R0402-LF). The speaker is connected to pin 17 (ALARM) and pin 8 (8P4R-470R0402-LF). The speaker is connected to pin 17 (ALARM) and pin 8 (8P4R-470R0402-LF).

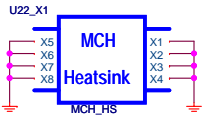
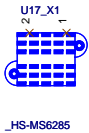
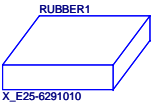
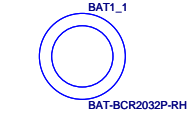
C199 C0.1U16V0402

Place near CK_48M_USB_ICh for EMI.

V_1P1_CORE
C305 C0.1U16Y040
Place near R643 for EMI.



Auto-BOM Manual Parts



ICH10

GPIO Pin	Type	Default	Function	Power	MUXED / UNMUXED	Pin-out
GPIO 0	I/O	GPI	BMBUSY# function, Pull-up to VCC3 with 10K	VCC3	MUXED	N7
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AK21
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 8.2K	VCC3		K6
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 8.2K	VCC3		L7
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 8.2K	VCC3		F2
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 8.2K	VCC3		G2
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AH22
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AK23
GPIO 8	I/O	GPI	Reserve for DDR_PEROK, Pull-up to VCC_DDR with 10K	VCC3_SB	UNMUXED	A20
GPIO 9	I/O	GPO/WOL	WOL_ENABLE/GPIO9, pull-down with 100K	VCC3_SB	MUXED	A18
GPIO 10	I/O	GPI	Detect AUDIO Devices, Pull-up to VCC3_SB with 10K	VCC3_SB	MUXED	C17
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		C16
GPIO 12	I/O	GPO	LAN_DISABLE	VCC3_SB	UNMUXED	A8
GPIO 13	I/O	GPI	SIO_PME# connect to SIO, pull-up VCC3_SB with 10K	VCC3_SB	UNMUXED	A19
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	A9
GPIO 15	I/O	GPO	PCI_STOP# for CK505 IAMT	VCC3_SB	MUXED	C15
GPIO 16	I/O	GPO	FAN switch, pull-up VCC3 with 10K.	VCC3	UNMUXED	M2
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AH21
GPIO 18	I/O	GPO	GTLREF GPO, Pull-up to VCC_DDR with 10K directly	VCC3	UNMUXED	K1
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AE20
GPIO 20	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	AF5
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AK25
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AJ24
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull-up VCC3 with 10K(Not Use)	VCC3	MUXED	J3
GPIO 24	I/O	NC		3.3V_SB	MUXED	A14
GPIO 25	I/O	GPO	CPU_STOP# for CK505 IAMT	3.3V_SB	UNMUXED	B18
GPIO 26	I/O	GPO	S4 STATE#	3.3V_SB		C11
GPIO 27	I/O	GPO	NC	3.3V_SB		A11
GPIO 28	I/O	GPO	NC	3.3V_SB		G18
GPIO 29	I/O	OC5#	OC#4 connect to USB connector	3.3V_SB		N1
GPIO 30	I/O	OC6#	OC#6 connect to USB connector	3.3V_SB		N5
GPIO 31	I/O	OC7#	OC#6 connect to USB connector	3.3V_SB		M1
GPIO 32	I/O	GPO	PROHOT# for NEC Economy mode	VCC3	UNMUXED	K2
GPIO 33	I/O	GPO	Pull-up to VCC3 with 4.7K through JC11 Jumper. (Default)	VCC3	UNMUXED	AF6
GPIO 34	I/O	GPO	NC	VCC3	UNMUXED	AH5
GPIO 35	I/O	GPO	Clear password	VCC3		L1
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE21
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE22
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AK24
GPIO 39	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH23
GPIO 40	I/O	OC1#	OC#0 connect to USB connector	3.3V_SB		N3
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	3.3V_SB		P7
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	3.3V_SB		R7
GPIO 43	I/O	OC4#	OC#4 connect to USB connector	3.3V_SB		N2
GPIO 44/45	I/O	OC8/9#	OC#6 connect to USB connector	3.3V_SB		P3/R6
GPIO 46/47	I/O	OC10/11#	OC#6 connect to USB connector	3.3V_SB		T7/P1
GPIO 48	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD20
GPIO 49	I/O	GPO	DMI strapping, pull-down 2.2K to GND	VCC3		AJ25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 2.7K	VCC5	MUXED	G13
GPIO 51	I/O	GNT1#	GNT1#	VCC5	MUXED	A7
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC5 with 8.2K	VCC5	MUXED	F13
GPIO 53	I/O	GNT2#	GNT2#	VCC3	MUXED	C7
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 2.7K	VCC5	MUXED	G8
GPIO 55	I/O	GNT3#	GNT3#(Not Use)	VCC3	MUXED	F7
GPIO 56	I/O	GPI	Clear password, pull-up to VCC3_SB with 10K.	3.3V_SB	MUXED	F16
GPIO 57	I/O	GPI	Pull-up to VCC3_SB with 10K directly for ME	3.3V_SB	MUXED	C12
GPIO 58	I/O	SPI_CS1	SPI_CS#(Not Use), SPI_CS1_F#(Not Use)	3.3V_SB	MUXED	F23
GPIO 59	I/O	OC0#	OC#0 connect to USB connector	3.3V_SB		P5
GPIO 60	I/O	LINKALERT	LINKALERT# pull-up to VCC3_SB with 10K	3.3V_SB		F18

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
Riser slot (PCI1)	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDR2 DIMM Configuration

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	SCLK_A0/SCLK_A0# SCLK_A2/SCLK_A2#
DIMM 2	0A4H	SCLK_B0/SCLK_B0# SCLK_B2/SCLK_B2#

SIO - SMSC-5617C Configuration

PIN NAME	PIN#	USAGE	Input/Output
GP41	77	SIO_PME#	OUTPUT
GP25	30	SMBCLK	INPUT
GP26	29	SMBCLK_ISO	INPUT
GP35	28	SMBDATA	OUTPUT
GP42	27	SMBDATA_ISO	OUTPUT

SMBus Distribution

SMBus	Power	Load
SMBCLK	VCC3_SB	SIO, ICH10, PCI EXPRESS[X16][X1]
SMBCLK_ISO	VCC3	DIMM, CLK GEN, MS7

Jumper Setting

JBAT1	(1-2)Normal	(2-3)Clear CMOS
JC11	(1-2)Normal	(2-3)ME Disable for FPROG
J1	(1-2)short: Normal	(1-2)Open: Clear PW

LGA775-CPU		
0.8375V - 1.6000V Core	-	84A
1.1V FSB Vtt	-	4.6A

Eaglelake (GMCH)		
1.1V FSB_VTT	-	1.2 A
1.1V Core TBD (USE LB)	-	13.8A
1.1V DMI/PCI Exp.	-	2.47 A
1.5V VCC_DDR	-	3.33A
1.5V VCC_SMCLK	-	350mA
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA
1.1V Vcc CL	-	4.3A

ICH10		
1.1V DMI	-	41 mA
1.1V Core	-	1.16A
1.5V_A USB/SATA/PLL	-	1.652A
1.5V_B PCI Exp.	-	0.646A
VCCRTC	-	6 uA
3.3V CL	-	19 mA
1.5V GbE LAN	-	87 mA
3.3V VccSus3_3	-	200mA
3.3V Vcc3_3	-	308mA
3.3V 10/100 LAN	-	19 mA
3.3V GbE LAN	-	1 mA
3.3V HDA	-	32 mA
3.3V SusHDA	-	33 mA

HD Audio ALC262VD		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

IDTCV184-2		
3.3V VDD_48/PCI/REF	-	250mA
0.3V-1V CPU/SRC/DOT/PLL	-	80mA

Boazman GbE		
3.3V_SB I/O & LED	-	15.5mA
1.8V AVDD	-	418.2mA
1.0V Core	-	277.2mA

ISL6334		
VCCP VRD11.1	-	0.8375V-1.6000V
3-Phase Switch	-	

W83310DS		
VTT_DDR	-	0.75V Linear 0.83A

MS11+ SW-Power		
VCC_DDR	-	1.5V PWM 13.86A

MS11+ SW-Power		
V_1P1_CORE	-	1.1V PWM 23.27A

MS7 Controller		
V_1P1_CL	-	1.1V Linear 3A

V_1P5_ICH		
1.5V Linear	-	2.385A

VCC3_SB		
3.3V Linear	-	3.96A

5VDUAL1		
5V Switch	-	4.367A

5VDIMM		
5V Switch	-	8.29A

DDRIII x2 & TERMINATOR		
0.75V VTT_DDR	-	1.2A
1.5V VCC_DDR (S0,S1)	-	3.6A
1.5V VCC_DDR (S3)	-	TBDmA

PCI Express x16 slot		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

AGP Extender riser slot		
	Luner Eagle	
+12V	-	1A
+5V	-	5.0A
+3.3Vaux	-	750mA
+3.3V	-	10.6A

PCI_E x1 slot		
+12V	-	0.5A
+3.3Vaux	-	375mA
+3.3V	-	3.0A

PCI slot		
+12V	-	0.5A
+3.3Vaux	-	375mA
+3.3V	-	7.6A
+5V	-	5.0A

USB x 8		
+5V (S0,S1)	-	4A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

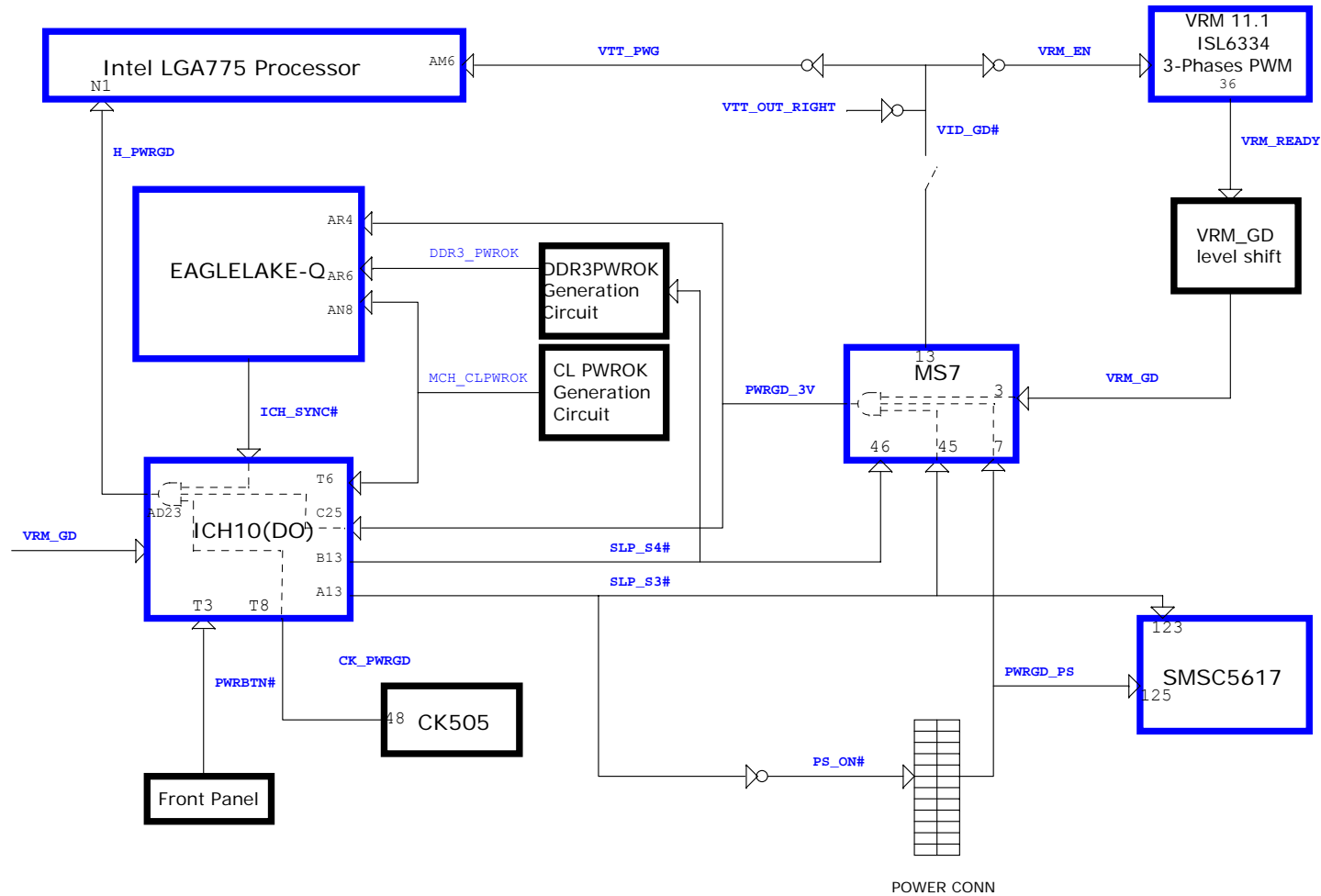
5VAudio
+5VR
500mA

3V
Battery


+12V
ATX
2x2

+5V +3.3V +5VSB +12V
ATX POWER

PWROK MAP



■MS-7420N1-970317.DSN.....Notes
1Remove R414,R415.....Have not used
2Delete R91.....Have not used
3short R84 immediately.....
4short R51 immediately.....
5short R271 immediately.....
6short R474 immediately.....
7C22,C27,C474,C476 0805 to 0603.....Unify the materials
8R156 change to 0402.....
9R67 change to 0805.....Unify the materials
10reserve C128.....RC timing
11Delete R246,C224,C209,C213,L14.....Have not used
12change C356 to 0.1U X7R.....Follow INTEL design
13C356,C366 change to X7R.....
14Remove R193,C166,Q32,R285,C239,Q43;add R183,R302;Add R474,R515 between RAM_DRY and 5V_DRV_F.....same Astoried-Z,ROPROS
15change Q59,Q63 to dualtype.....
16Reserve R51Intel suggestion
17R493,R495 change to VTT_OUT RIGHT.....Due to layout route and follow INTEL design update
18Empty R310,R303.....INTEL design update
19Add JLPC1 debug circuit.....For debug ,MP remove
20Change GMCH from A0 steepig to A2 steping.....
21Remove R333.....GPIO18 is already output function,don't need to pull-up.
22change COM2(SPI debug port) power source to V_3P3_CL.....update to same the SPI ROM (U15) power source
23Delete R357.....Have not used
24Delete R281,R282Have not used
25Remove EC29.....V_1P1_CORE power ripple noise OK
26Delete EC54.....Have not used
27Delete EC62,Add C438,EC63 stuff.....VCC_DDR ,VTT_DDR power ripple noise OK
28Delete INTR1.....Have not used
29Add C552,change CHOKE2,CHOKE7,CHOKE8 to 0.5uH,chane R90,R73,R112 to 9.09K,change C76 to 470P,R65 to 1.69K.....For transient ,efficiency and load line
30update U14 library,reserve R137,add C209 1uF.....
31Remove Q40,R272.....INTEL PSI# design update
32Reserve Q59Substitute Q39 circuit ,Verification when getting latest CPU
33Add level shift between PROCHOT# and ICH10 pinK2(GPIO32).....For NEC ENCONOMY MODE
34Delete R94 and add D23.....Due to Peci_REQUEST have electric leakage ,SMSC have workaroud to add a diode to avoid.
35change C145,C311,C317 to 1U 0805 X7R.....Unify the materials
36L20 change to 0ohm ,delete R343.....noise OK
37update L25,L18 description.....
38Delete C156,C169,C178.....For EMI request
39C158,C171,C179,C161,C174,C182 change to 5.6P,Add C49C50,C51,C53For EMI
40Add C530 ,C436,C473 to 0.01U;Add C450 to 0.1uF.....For EMI
41Change Q69,Q70 to daul type,delete R488.....Unify the materials
42Stuff R392.....support danbury tec.
■MS-7420N1-970317_B.DSN
43Stuff R269,R51,C345,Remove Q90.....Use ICH10 DRAMPWROK function pin.
44Cahnge E33,EC31,EC29 to EL cap 1800uFfor dynamic load(24A) overspec.
45C117,C118 change to 47P.....for crystall (accuracy),next version change to SMT type 20ppm.
46R283,R584 change to 1.02K.....finetune VCC_DDR,V_1P1_CORE POWER
47EC52 change to 1800u(EL).....for dynamic load(3A) overspec.
48F_USB1 change to new connector.....F_USB1 change to new connector (pin length is 4.0 mm)

 MICRO-START INTL CO.,LTD.		
Title		
History		
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